54.10 Protocol Implementation Conformance Statement (PICS) proforma for Clause 54, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4[2]

54.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 54, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

54.10.2 Identification

54.10.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

54.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ak-2004, Clause 54, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ak-2004.)	

Date of Statement	

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

54.10.3 PICS proforma tables for 10GBASE-CX4 and baseband medium

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	54.9		M	Yes [ ]

54.10.4 Major capabilities / options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII interface	46, 54.1	Interface is supported	O	Yes [ ] No [ ]
XGXS	XGXS and XAUI	47, 54.1		O	Yes [ ] No [ ]
PCS	Support of 10GBASE-X PCS / PMA	48, 54.1		O	Yes [ ] No [ ]
DC	Delay constraints	54.3	Delay no more than 512 BT or 1 pause_quantum	M	Yes [ ]
*MD	MDIO capability	54.4	Registers and interface supported	O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

54.10.4.1 PMD Functional specifications

Item	Feature	Sub clause	Value/Comment	Status	Support
PF1	Transmit function	54.5.2	Convert the four logical signals requested by PMD_UNITDATA.request (tx_bit<0:3>) to 4 electrical signals	M	Yes [ ]
PF2	Delivery to the MDI	54.5.2	Supplies four electrical signal streams for delivery to the MDI	M	Yes [ ]
PF3	Mapping between logical signal and electrical signal for transmitter	54.5.2	A positive differential voltage is a one	M	Yes [ ]
PF4	Transmit Signal order	54.5.2	PMD_UNITDATA.request (tx_bit<0:3>) = (SL0<p>/<n>, SL1<p>/<n>, SL2<p>/<n>, SL3<p>/<n>)	M	Yes [ ]
PF5	Receive function	54.5.3	Convert the four electrical signals received from the MDI to 4 logical signals PMD_UNITDATA.indicate(rx_bit<0:3>) per 54.6.4	M	Yes [ ]
PF6	Mapping between electrical signal and logical signal for receiver	54.5.3	A positive differential voltage is a one	M	Yes [ ]
PF7	Receive Signal order	54.5.3	(DL0<p>/<n>, DL1<p>/<n>, DL2<p>/<n>, DL3<p>/<n>) = PMD_UNITDATA.indicate (rx_bit<0:3>)	M	Yes [ ]
PF8	Global PMD Signal Detect function	54.5.4	Report state via PMD_SIGNAL.indicate (SIGNAL_DETECT)	M	Yes [ ]
PF9	Global PMD Signal Detect OK threshold	54.5.4	SIGNAL_DETECT = OK for signal value >= 175 mV for at least 1 UI on each of the four lanes	M	Yes [ ]
PF10	Global PMD Signal Detect FAIL threshold, minimum	54.5.4	SIGNAL_DETECT = FAIL not asserted for signal level < 50 mV for < 250 μs on all four lanes	M	Yes [ ]
PF11	Global PMD Signal Detect FAIL threshold, maximum	54.5.4	SIGNAL_DETECT = FAIL asserted for signal level < 50 mV for > 500 μs on any of the four lanes	M	Yes [ ]
PF12	Global_PMD_transmit_disable	54.5.6	Disables all transmitters by forcing a constant output state	O	Yes [ ] No [ ]
PF13	PMD_fault disables transmitter	54.5.6	Disables all transmitters by forcing a constant output state when a fault is detected	O	Yes [ ] No [ ]
PF14	Effect on loopback of Global_PMD_transmit_disable	54.5.6	Global_PMD_transmit_disable does not affect loopback function	M	Yes [ ]

Item	Feature	Sub clause	Value/Comment	Status	Support
PF15	PMD_transmit_disable_n	54.5.7	Disables transmitter n (n=0:3) by forcing a constant output state	O	Yes [ ]
PF16	PMD_fault disables transmitter n	54.5.7	Disables transmitter n (n=0:3) by forcing a constant output state when a fault is detected	O	Yes [ ] No [ ]
PF17	Effect on loopback of PMD_transmit_disable_n	54.5.7	PMD_transmit_disable_n does not affect loopback function	M	Yes [ ]
PF18	Loop Back	54.5.8	Loopback function provided	M	Yes [ ]
PF19	Transmitters on during loopback	54.5.8	Loopback function does not disable the transmitters	M	Yes [ ]

54.10.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Lane-by-Lane Signal Detect function	54.5.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of 54.5.4	MD:M	Yes [ ] N/A [ ]
MF2	PMD_fault function	54.5.9	Sets PMD_fault to a logical 1 if any local fault is detected otherwise set to 0	MD:M	Yes [ ] N/A [ ]
MF3	PMD_transmit_fault function	54.5.10	Sets PMD_transmit_fault to a logical 1 if a local fault is detected on the transmit path otherwise set to 0	MD:M	Yes [ ] N/A [ ]
MF4	PMD_receive_fault function	54.5.11	Sets PMD_receive_fault to a logical 1 if a local fault is detected on the receive path otherwise set to 0	MD:M	Yes [ ] N/A [ ]

54.10.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Meets specifications at TP2	54.6.3		M	Yes [ ]
DS2	Test load	54.6.3.2	100 Ω differential load with return loss > 20 dB	M	Yes [ ]
DS3	Signaling speed	54.6.3.3	3.125 GBd ± 100 ppm	M	Yes [ ]
DS4	Maximum transmitter differential peak-to-peak output amplitude	54.6.3.4	Less than 1200 mV	M	Yes [ ]
DS5	Minimum transmitter differential peak-to-peak output amplitude	54.6.3.4	Greater than 800 mV	M	Yes [ ]
DS6	Maximum transmitter differential peak-to-peak amplitude difference	54.6.3.4	Less than 150 mV	M	Yes [ ]
DS7	Common mode output voltage	54.6.3.4	Between –0.4 V and +1.9 V	M	Yes [ ]
DS8	Transmitter output return loss	54.6.3.5	Per Equation (54–1) and Equation (54–2)	M	Yes [ ]
DS9	Transmitter output return loss reference impedance	54.6.3.5	100 Ω	M	Yes [ ]
DS10	Transmitter output template test pattern	54.6.3.6	Per 48A.2	M	Yes [ ]
DS11	Transmitter output template compliance	54.6.3.6	Met while connected to test fixture shown in Figure 54–3, with all outputs active	M	Yes [ ]
DS12	Transmitter output normalization	54.6.3.6	Per process defined in 54.6.3.6	M	Yes [ ]
DS13	Transmitter output template	54.6.3.6	Lies within template of Figure 54–6 and Table 54–4	M	Yes [ ]
DS14	Rising edge transition time	54.6.3.7	Between 60 ps and 130 ps as measured per 54.6.3.7	M	Yes [ ]
DS15	Falling edge transition time	54.6.3.7	Between 60 ps and 130 ps as measured per 54.6.3.7	M	Yes [ ]
DS16	Jitter requirements	54.6.3.8	Meet BER bathtub curve, See Annex 48B	M	Yes [ ]
DS17	Transmit jitter, peak-to-peak	54.6.3.8	Meet BER bathtub curve, See Annex 48B, with Total jitter < 0.35 UI Deterministic jitter < 0.17 UI Random jitter < 0.27 UI	M	Yes [ ]
DS18	Jitter test patterns	54.6.3.9	As per Annex 48A.5	M	Yes [ ]

54.10.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RS1	Bit Error Ratio	54.6.4.1	BER of better than 10^{-12}	M	Yes [ ]
RS2	Signaling speed	54.6.4.2	3.125 GBd ± 100 ppm	M	Yes [ ]
RS3	AC Coupling	54.6.4.3	—	M	Yes [ ]
RS4	Input peak-to-peak amplitude tolerance	54.6.4.4	Accepts signals compliant with 54.6.3, may be larger than 1200 mV	M	Yes [ ]
RS5	Receiver input return loss	54.6.4.5	Per Equation (54–1) and Equation (54–2)	M	Yes [ ]

54.10.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Differential reference impedance	54.7.1	100 Ω	M	Yes [ ]
CA2	Insertion loss	54.7.2	Per Equation (54–3)	M	Yes [ ]
CA3	Return loss	54.7.2	Per Equation (54–4), Equation (54–5), and Equation (54–6)	M	Yes [ ]
CA4	NEXT	54.7.4.1	Per Equation (54–6)	M	Yes [ ]
CA5	MDNEXT	54.7.4.2	Per Equation (54–7)	M	Yes [ ]
CA6	ELFEXT	54.7.5.1	Per Equation (54–9)	M	Yes [ ]
CA7	MDELFEXT	54.7.5.2	Per Equation (54–10)	M	Yes [ ]
CA8	Shielding	54.7.6	Class 2 or better in accordance with IEC 61196-1	M	Yes [ ]
CA9	Crossover function	54.7.7	Per Figure 54–11	M	Yes [ ]
CA10	Cable assembly connector type	54.8.1	IEC 61076-3-113 latch-type plug	M	Yes [ ]
CA11	MDI connector type	54.8.1	IEC 61076-3-113 latch-type receptacle	M	Yes [ ]
CA12	Pin assignments	54.8.2	Per Table 54–7	M	Yes [ ]