

## IEEE Test Interface (STIL) and Memory Core Test Language - IEEE 1450(TM) Series (Bundle)

Extensions to the test interface language (contained in this bundle) are defined that (1) facilitate the use of the language in the design environment and (2) facilitate the use of the language for large designs encompassing subdesigns with reusable patterns. Examples of the DC conditions for device power supplies are: device power supply setup, power sequencing to the device and power supply limit. Although native STIL data are tester independent, the actual process of mapping the test program onto tester resources may be critical, and it is necessary to be able to completely and unambiguously specify how the STIL programs and patterns are mapped onto the tester resources. TRC (which stands for either tester resource constraints or tester rules checking, depending on the usage) is an extension to the STIL language to facilitate this operation. In an SoC flow, the smaller design embedded in the larger design is commonly called a core and the larger design is commonly called the SoC. The core is a design provided by a core provider, and the task of incorporating the sub-design into the SoC is called Core System Integration. It facilitates the development and reuse of test and repair mechanisms for memories. It defines constructs that represent the test structures internal to the memory core for reuse in the creation of the tests for the logic outside the memory core. Semantic rules are defined for the language to facilitate interoperability between different entities (the memory core provider, the system integrator, and the automation tool developer) involved in the creation of an SoC. The capabilities are an extension of IEEE Std 1450.6(TM)-2005. As a result of this extension, CTLs limitations of handling memories are addressed.

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- IEEE 1450-1999
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