Interpretation Number: 1-11/04 (Annex G acccuracy)
Topic: Accuracy of material in Annex G
Relevant Clauses: Annex G
Classification: Conflicts with clause 17

Interpretation Request

1.Designation of the standard, including the year of publication.
IEEE Std 802.11a-1999
Part 11: Wireless LAN Medium Access Control (MAC) and Pjysical Layer (PHY) specifications
High-speed Physical Layer in the 5 GHz Band

2.The specific subsection being questioned.
Annex G.
An example of encoding a frame for OFDM PHY. Table G.17-Last 144 bits scrambling.

3. The applicable conditions for the case in question.

In order to check if our design of the PHY is correct, we have check it by means of the example given in Annex G - "An example of encoding a frame for OFDM PHY".

All our results match properly with those given in all the tables except for Table G.17 - “Last 144 bits after scrambling.” In this case, the bits number 818 and 820 that are in the standard are '0'. However, we obtain two '1'.

In order to check if the scrambler module works properly we have try to obtain the 127-bit repeatitive sequence given in page 16 in 17.3.5.4 - “PLCP DATA scrambler and descrambler” and we did it correctly. As it can be seen, the values of the 7-bit shift register of the scrambler depends only on the seed. In the example given, the seed is '1011101' and we have checked as well that we match the Table G.15- “Scrambling sequence for seed 1011101.” Therefore, in our opinion the mismatch in 'Table G.17' might be caused by the input of the scrambler, that is, the DATA bits. However, we are obtaining the same values than those given in Table G.14- “Last 144 DATA bits.”

Could you confirm that the data shown in 'Table G.17' is completely correct?

- The two bits (bit#818 and bit#820) in the Table G.17 should be corrected.
  - Both of bit #818 and bit #820 in the Table G.17 are “0” in current standard.
  - Both bit #818 and bit #820 should be modified to be “1”.
- Table G.1:
  - Table G.1 consists of following items.
    - The MAC header (24 octets)
    - The first 72 characters of the original message converted to ASCII code
    - The CRC32 (4 octets)
  - A PSDU of length 100 octets (= 800 bits)
    - {04 02 00 2e 00 60 08 cd … 74 72 65 61 da 57 99 cd}
- Generation of DATA field in PPDU frame:
  - The DATA field in a PPDU frame consists of SERVICE field, PSDU, tail (PPDU TAIL) and Pad bits.
  - Table G.13 shows the first 144 bits of the DATA field.
    - The SERVICE field (sixteen “0” bits) are added before PSDU.
  - Table G.14 shows the last 144 bits of the DATA field.
    - Assuming the modulation mode of 36M bps (16QAM, r=3/4), 42 Pad bits are appended in this case.
- Table G.15 – Scrambling sequence for seed 1011101
  - This is the output sequence of the scrambler when the initial value of the shift register is 1011101.
  - We have confirmed that the Table G.15 was correct.
- We have confirmed that:
  - Table G.16 (First 144 bits after scrambling) was correct.
  - Table G.17 (Last 144 bits after scrambling) was NOT correct as the requester pointed out.

Table G.17

##	Bit	##	Bit	##	Bit	##	Bit	##	Bit	##	Bit
720	0	744	0	768	1	792	0	816	0	840	0
721	1	745	0	769	0	793	0	817	0	841	0
722	1	746	0	770	1	794	1	818	**1**	842	0
723	1	747	1	771	0	795	1	819	0	843	0
724	1	748	0	772	0	796	0	820	**1**	844	1
725	1	749	1	773	0	797	0	821	0	845	1
726	0	750	1	774	0	798	0	822	0	846	1
727	1	751	1	775	0	799	0	823	0	847	0
728	1	752	0	776	1	800	1	824	1	848	1
729	0	753	0	777	1	801	0	825	1	849	1
730	0	754	1	778	1	802	0	826	0	850	1
731	0	755	1	779	0	803	0	827	1	851	1
732	1	756	1	780	1	804	1	828	1	852	0
733	0	757	0	781	1	805	1	829	1	853	0
734	1	758	0	782	0	806	0	830	0	854	1
735	0	759	1	783	0	807	0	831	0	855	0
736	0	760	0	784	0	808	1	832	0	856	1
737	0	761	0	785	0	809	1	833	1	857	1
738	1	762	0	786	1	810	0	834	1	858	0
739	0	763	1	787	0	811	0	835	1	859	0
740	0	764	0	788	1	812	1	836	1	860	1
741	1	765	1	789	0	813	0	837	1	861	0
742	1	766	0	790	0	814	1	838	1	862	0
743	1	767	1	791	0	815	0	839	1	863	1

Data	Tail	Pad

- The bit #818 and bit #820 in the Table G.17 correspond to the PPDU TAIL bits.
- The PPDU TAIL bits and PAD bits are all “0”
  - There will be exact sequence of the scrambler output after bit #816 in the Table G.17.
  - The bits #818 and #820 in the Table G.17 correspond the bits #56 and #58 in the Table G.15 which have value of “1”.

The conclusion of this analysis is that two bits in table G.17 are in error. This error will be brought to the attention of the 802.11 working group to be addressed in the next revision of the standard.