Agenda

• Introduction to ESD

• SEED Simulation for robust system design

• Multigigabit Ethernet

• Conclusion and Outlook
Automotive mega trends shaping IVNs
ESD protection fulfilling ISO norms exceeding AEC-Q101 qualification

ESD protection in various footprints and packages for classic in-vehicle networks

Investment in R&D with focus on innovative high-speed solutions

- LIN
- CAN-FD/XL
- 10BASE-T1S
- 100BASE-T1
- 1000BASE-T1
- MGBASE-T1
- SerDes
- USBx
- HDMIx
- ILaS
- 5G

From classic flat wiring harness to ...

... modern domain and future zonal architecture
Automotive Compliance Testing

Environmental Testing
- Life Profile
- Mechanical
- Climate
- Chemical
- ...

Electrical Testing
- Functional
- Board net Pulses
- EMC
- ESD (e.g. IEC61000-4-2)
- ...

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ESD – Electro Static Discharge

**WHAT**
A sudden discharge between persons, devices or components

**HOW**
- A charged person touches an integrated circuit (IC)
- An electrostatic field is induced by high voltages
- A charged IC drops on a grounded metal plate
- A charged machine touches an IC

**PROBLEM**
- Causing malfunction (reversible by power-off-on cycle)
- Destruction of electrical components (irreversible): gate oxide, metallisation or PN junctions
New IC requirements shape ESD threat

MEGA TRENDS

Connected & Autonomous
Electrified
Shared Mobility

Gate thickness [nm]

ESD area to achieve 2 kV HBM

IC ESD robustness decreases!

IC area

ESD area >> IC design space

Source: ESDA, 2016; IEEE, 2012; Duvvy/Miller, 2009

Rel. ESD design costs

That requires dedicated system-level ESD solutions!
ESD protection directly at the connector to keep the ESD currents off the PHY

+ Decoupling of IC int. from ext. ESD protection
+ Best overall system ESD performance

ESD protection at the IC pins
- Potential mismatch of int. and ext. ESD protection (dual sourcing can be critical)
- No protection of passive components
OPEN Alliance Spec. for ESD protection devices

General requirements

General requirements for 100/1000BASE-T1

- Trigger voltage > 100V, $V_{DC,max} > 24V$
- Bi-direction device, 15kV IEC, 1000 discharges

ESD discharge current measurement

- Quantification of the current that would flow into the PHY

Additional tests:

- Mixed mode S-parameter measurements
  - To evaluate transmission, symmetry, and mode conversion, replaces requirements on $C_p$ and matching

- Damage from ESD
  - To verify degradation, first measure S-parameters, apply ESD (8kV) discharges, and check S-parameters again

- Unwanted clamping
  - Evaluate impact of ESD device onto RF immunity testing
Proof of Concept via measurements
Determines the residual current flowing into IC (PHY) during an ESD event

ESD Gun Test on PCB (acc. IEC61000-4-2)

Contact discharge 4kV (6kV)

ESD Protection pass/fail?

Evaluation of IC current limits acc. HBM
Idea of System Efficient ESD Design (SEED)
System modelling for transient system-level ESD analysis via simulation

- Evaluation of currents into IC during ESD event
- Prediction of System-level ESD Robustness
- System improvement using Virtual Prototyping
- Reduction of engineering loops (time & cost)
Model Types Applied to Realise the SEED Model

- Behavioural dynamic model
- Equivalent circuit based model
- Network of lumped elements

ESD-Gun
ESD-Protect
CMT
De-Caps
CMC
IC
System PCB
Modelling of ESD Generator

1 kV discharge in 2 Ohm Pellegrini Target (acc. IEC 61000-4-2)

- Entire shape of ESD generator model is replicated with very high precision and corresponds to IEC61000-4-2

The extended ESD generator model used here, is based on paper: S.Yang et al., “Effect of Different Load Impedances on ESD Generators and SPICE Models”, IEEE 2017
Modelling of ESD Protection Device

Fully dynamic model of the ESD Protection Device

The extended dynamic model used here, is based on paper: P. Wei et al., “TVS Transient Behavior Characterization and SPICE-Based Behavior Model”, 40th EOS/ESD Symposium, 2018

- The ESD Protection is modeled using TLP. Not only the static behavior is modeled but also the dynamic behavior using peak voltages of each TLP pulse.
Modelling of CMC
Simulation fits well the measurements

The CMC Protection is modeled using TLP measurement similar to the modeling of the ESD device.
IC Current after ESD Generator Pulse of 4kV

Current into IC

S.Bub, et al., “Efficient prediction of ESD discharge current according to OPEN Alliance 100BASE-T1 specification using SEED”, White Paper, 2020

Good match between simulation and measurement.
Summary SEED Simulation

- SEED predicts rest currents into the IC for direct ESD injection

- System Model can be also extended for transient analysis of coupled ESD injections
Application overview: capacitance vs. datarate

High-speed requires low capacitance
High performance package approaches: FCLGA

Package technology is essential for signal integrity.

- Signal Integrity
- High Performance
- SI Improved Package Technology
- Molding Compound
- Die (flip-chip mounted)
- Redistribution Layer (RDL) of Substrate
- Solder Mask Layer
- Side Wettable Flank
- Laminate Substrate

- $C_D > 50 \text{ pF}$
- $30 \text{ pF}$
- $10 \text{ pF}$
- $1 \text{ pF}$
- $0.5 \text{ pF}$

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## Multigigabit Ethernet: Possible ESD Circuitry

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### Electrical Performance

- **V_{h} = 60V**
- **V_{t} = 100V**

- **V_{h} = 2.5V**
- **V_{t} = 12V**

- **V_{h} = 2.5V**
- **V_{t} = 12V**

### CMC

- **~µH Range**
- **~nH Range**
- **--**

### Benefits

- **ESD Performance**
  - All circuitry is protected
  - HV Boardnet 48V
  - PoDL - ready
  - EM immunity
- **Best clamping**
  - ESD and EMI
- **Low cost**
  - SI Performance

Plus further application & quality requirements e.g. 2x AEC-Q101 / T_{j} = 175 °C
Conclusion & Outlook
More on nexperia.com

Automotive Trends
- Electrification
- Connectivity
- Autonomous Driving

Efficiency through Simulations

Summary SEED Simulation
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New requirementes – new solutions
EFFICIENCY WINS.