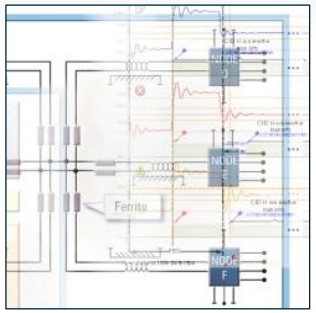
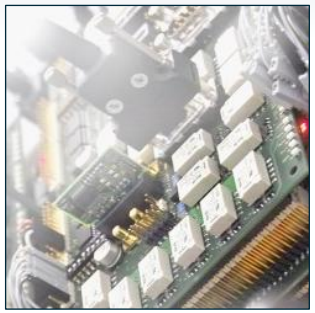





10BASE-T1S In-Vehicle Network Validation

Testing of the physical layer as defined by the IEEE standard, possible extensions and MPoE

October 15th, 2025

Presentation by

C&S group GmbH – Patrick Isensee

TDK Electronics AG – Thomas Schamberger

10BASE-T1S In-Vehicle Network Validation

Agenda

1. IVN Validation of the Physical Layer
    a. 10BASE-T1S in the Past and Present Day
    b. Simulation! Why?
    c. Validation Criteria
2. Point of Investigation
    a. Impact of MPoE on the Signal Integrity in a Multidrop Bus System
    b. Power Management in MPoE
    c. Challenge of MPoE – DMI vs. Single Inductors
3. Conclusion and next steps

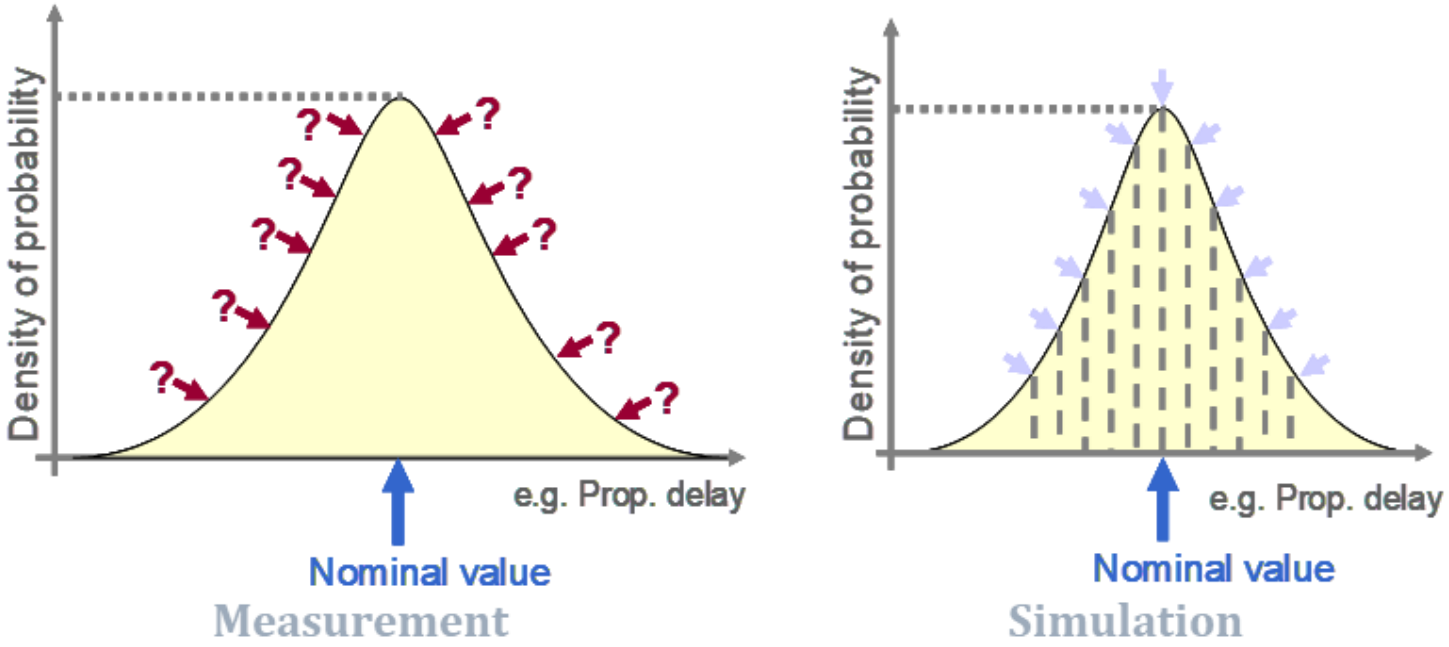
10BASE-T1S In-Vehicle Network Validation

Why 10BASE-T1S?

- A lower speed grade and a multidrop system with efficient PLCA meet the requirements of new E/E zonal architectures, with the goal of achieving SDV (Software-Defined Vehicle) in conjunction with RCP (Remote Control Protocol) and MACsec (Media Access Control Security)
- Significant cost reduction due to PMD implementations and MPoE
- The potential for extending the design of topologies to encompass layouts that have not been covered in the IEEE

10BASE-T1S In-Vehicle Network Validation

Why is IVN simulation so important?



- Quality assurance
- Total cost reduction
- Short development time
- Broader analysis compared to laboratory tests incl. worst-case conditions

Simulation is the most important phase during the validation process of today's complex topologies

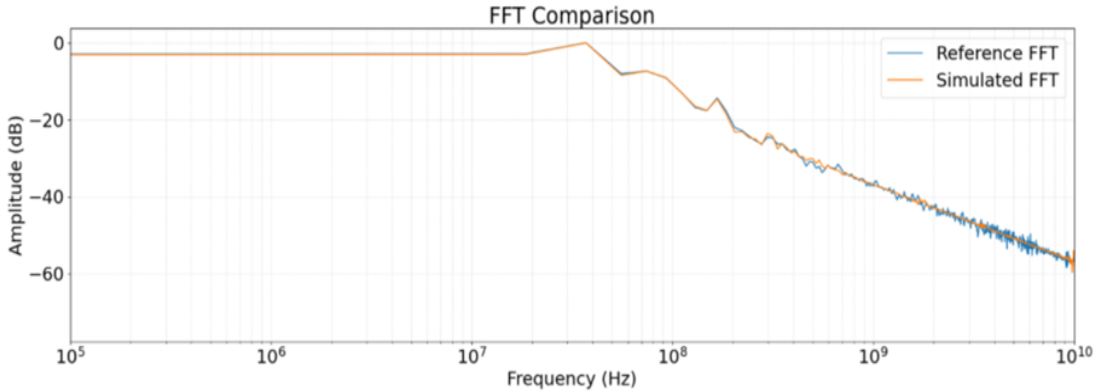
10BASE-T1S In-Vehicle Network Validation

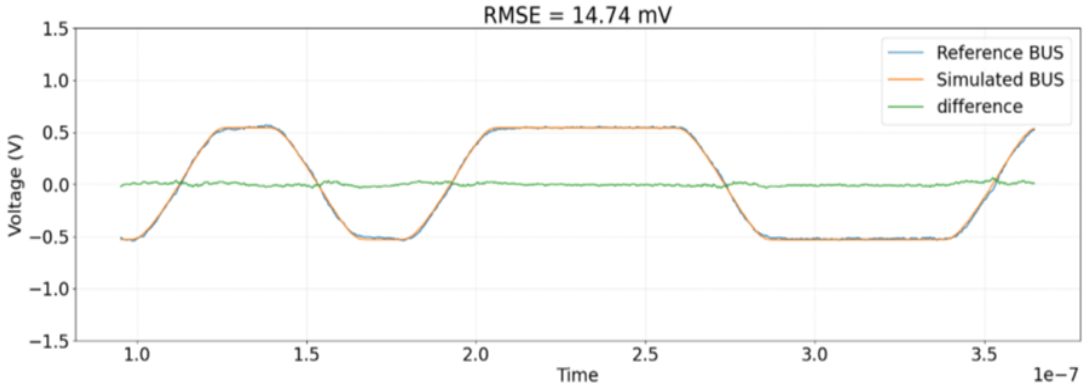
The challenge of realistic and precise simulation models

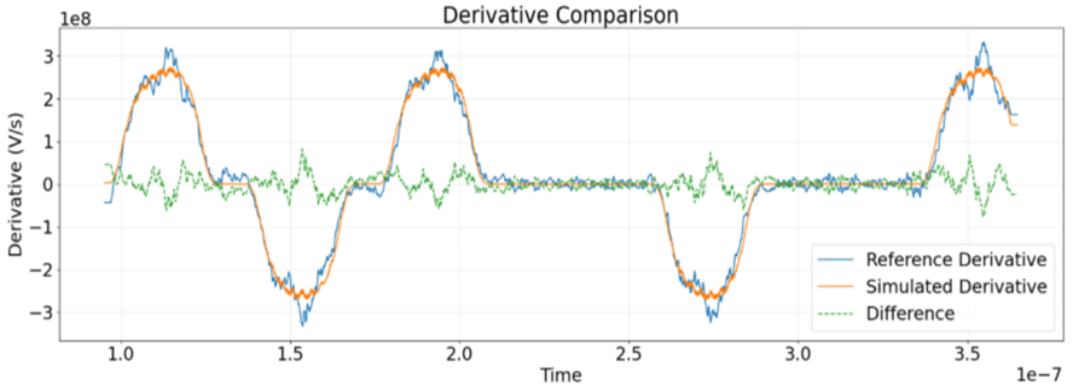
Model development process

Model development

Topology verification

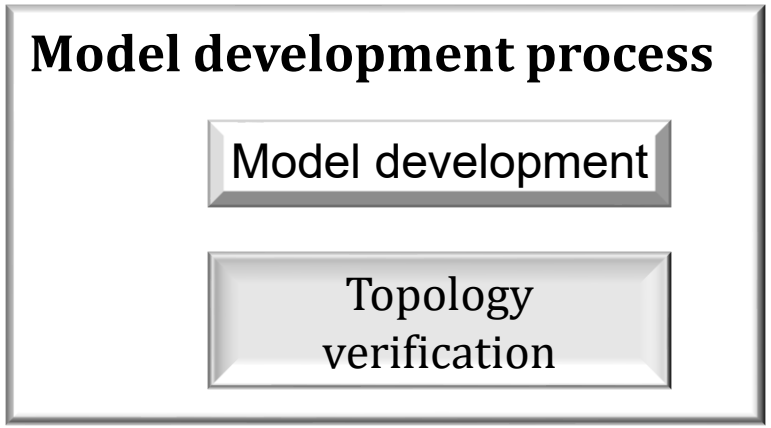


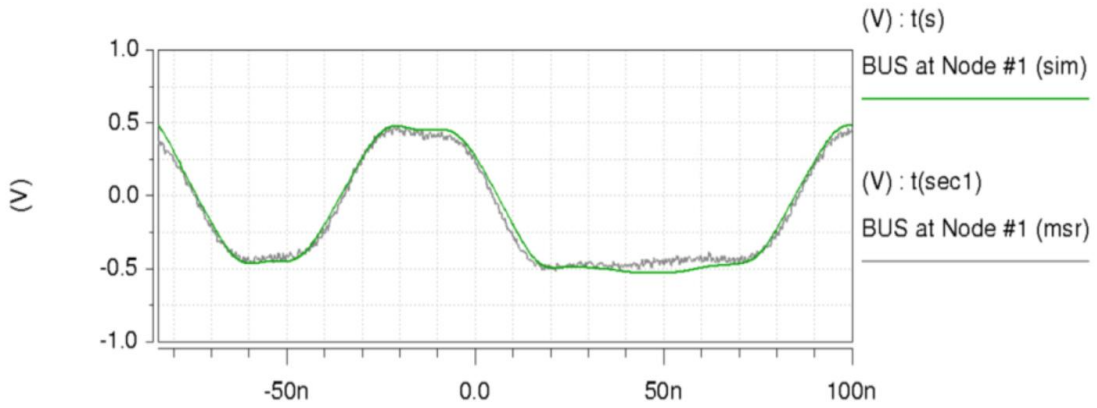


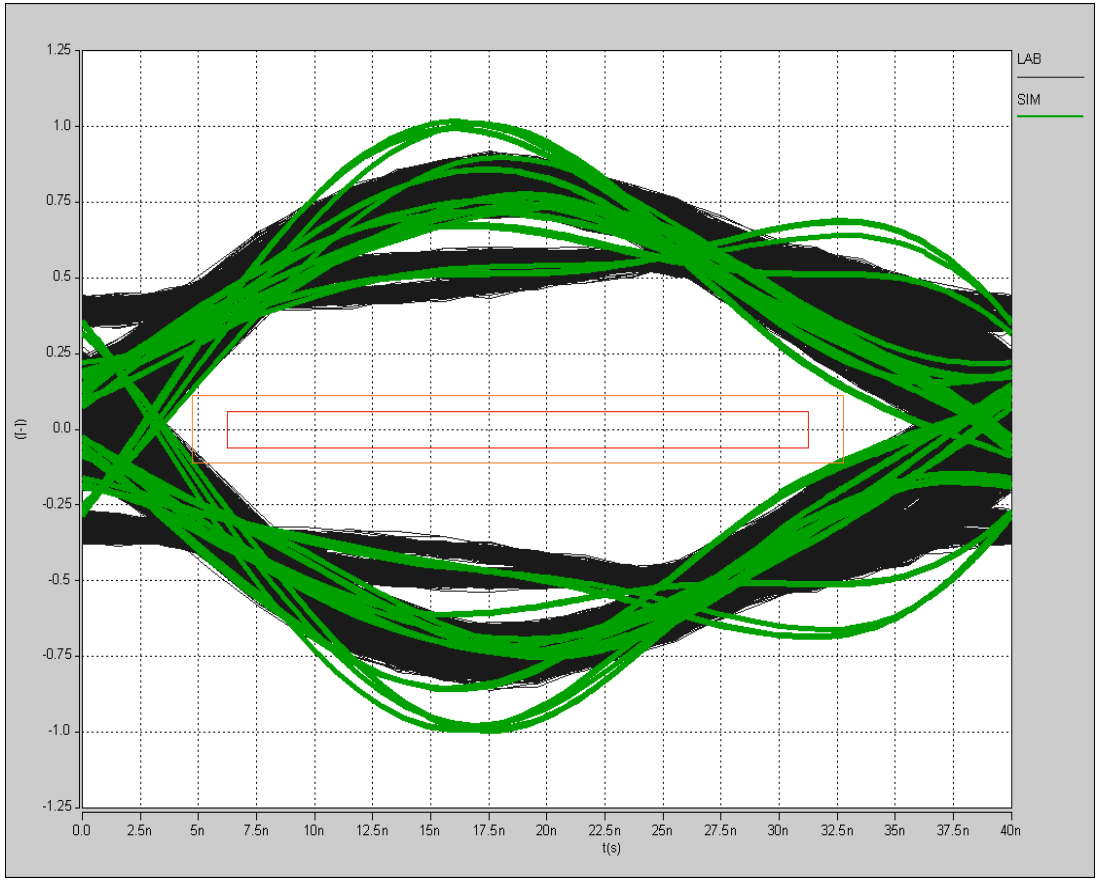


10BASE-T1S In-Vehicle Network Validation

The challenge of realistic and precise simulation models



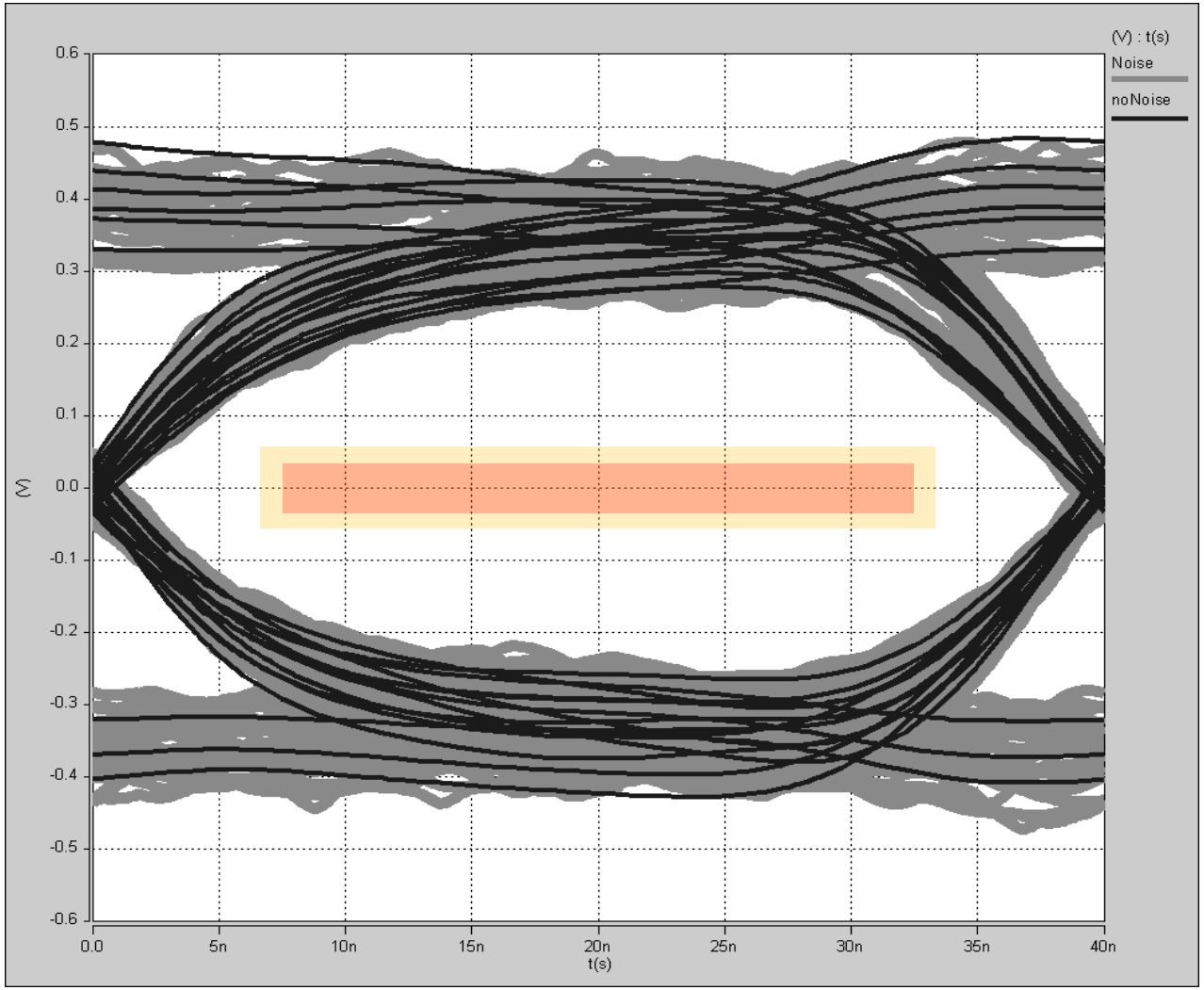




10BASE-T1S In-Vehicle Network Validation

Physical layer validation

- Eye diagram as defined in OPEN Alliance system implementation
  - ±30 mV and ≥25 ns mask
  - First implementations could have extended mask limits to increase robustness and gain experiences
    - » Include a further WARNING mask
    - » Run an initial simulation with noise injection (generally 200 mVpp) and increase the OPEN Alliance mask limits accordingly

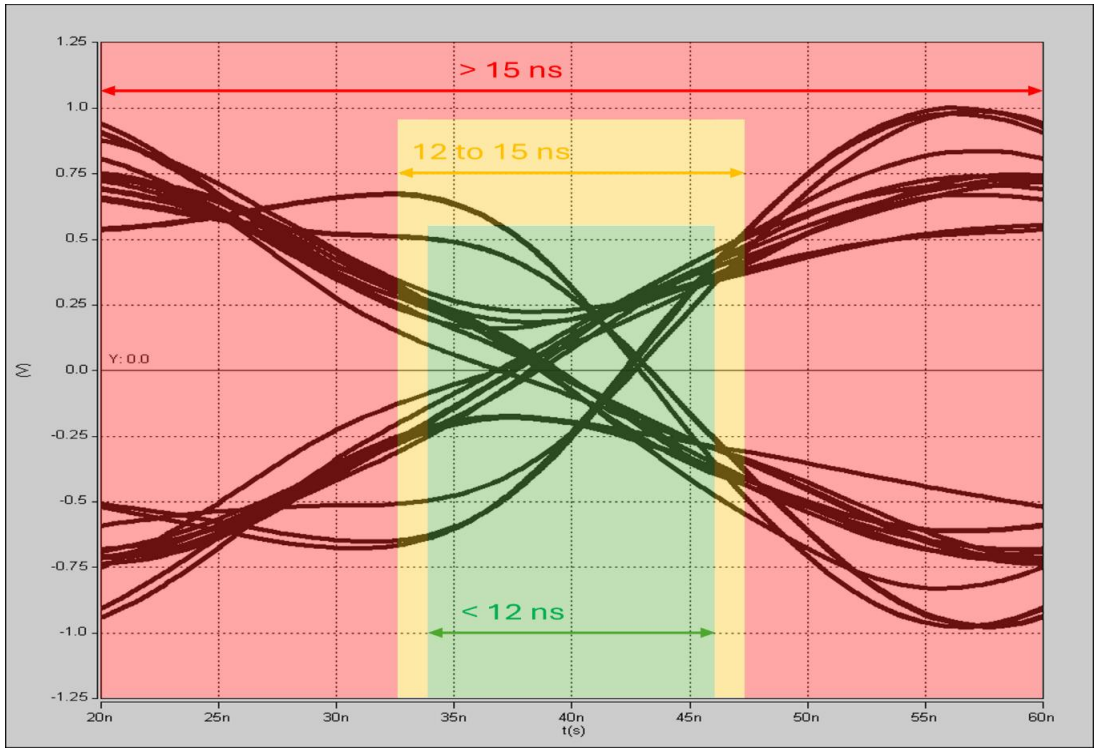


Note:
Several verification measurements have shown that 10BASE-T1S PHYs are very robust and could work with a very noisy signal without any problem.

10BASE-T1S In-Vehicle Network Validation

Physical layer validation

- Informative criteria for an extended view of the test engineer
  - Jitter
  - Heat maps



Jitter

Transmitter	Receivers					
	ECU1	ECU2	ECU3	ECU4	ECU5	ECU6
ECU1		1.228 [ns]	1.250 [ns]	4.566 [ns]	2.167 [ns]	898.000 [ps]
ECU2	1.234 [ns]		925.000 [ps]	6.651 [ns]	1.932 [ns]	1.777 [ns]
ECU3	1.167 [ns]	897.000 [ps]		7.297 [ns]	1.834 [ns]	1.932 [ns]
ECU4	2.950 [ns]	1.990 [ns]	2.097 [ns]		1.851 [ns]	1.257 [ns]
ECU5	1.068 [ns]	911.000 [ps]	1.035 [ns]	2.002 [ns]		1.733 [ns]
ECU6	1.376 [ns]	2.637 [ns]	2.743 [ns]	1.757 [ns]	3.332 [ns]	

Eye width

Transmitter	Receivers					
	ECU1	ECU2	ECU3	ECU4	ECU5	ECU6
ECU1		38.772 [ns]	38.750 [ns]	35.434 [ns]	37.833 [ns]	39.102 [ns]
ECU2	38.766 [ns]		39.075 [ns]	33.349 [ns]	38.068 [ns]	38.223 [ns]
ECU3	38.833 [ns]	39.103 [ns]		32.703 [ns]	38.166 [ns]	38.068 [ns]
ECU4	37.050 [ns]	38.010 [ns]	37.903 [ns]		38.149 [ns]	38.743 [ns]
ECU5	38.932 [ns]	39.089 [ns]	38.965 [ns]	37.998 [ns]		38.267 [ns]
ECU6	38.624 [ns]	37.363 [ns]	37.257 [ns]	38.243 [ns]	36.668 [ns]	

Eye height

Transmitter	Receivers					
	ECU1	ECU2	ECU3	ECU4	ECU5	ECU6
ECU1		524.335 [mV]	542.323 [mV]	443.301 [mV]	500.790 [mV]	382.591 [mV]
ECU2	585.912 [mV]		336.451 [mV]	404.528 [mV]	452.758 [mV]	418.482 [mV]
ECU3	591.018 [mV]	355.362 [mV]		370.050 [mV]	456.129 [mV]	417.021 [mV]
ECU4	482.625 [mV]	472.474 [mV]	458.053 [mV]		397.274 [mV]	364.390 [mV]
ECU5	525.616 [mV]	430.122 [mV]	448.069 [mV]	348.794 [mV]		577.139 [mV]
ECU6	423.824 [mV]	383.323 [mV]	400.370 [mV]	617.723 [mV]	529.074 [mV]	

10BASE-T1S In-Vehicle Network Validation

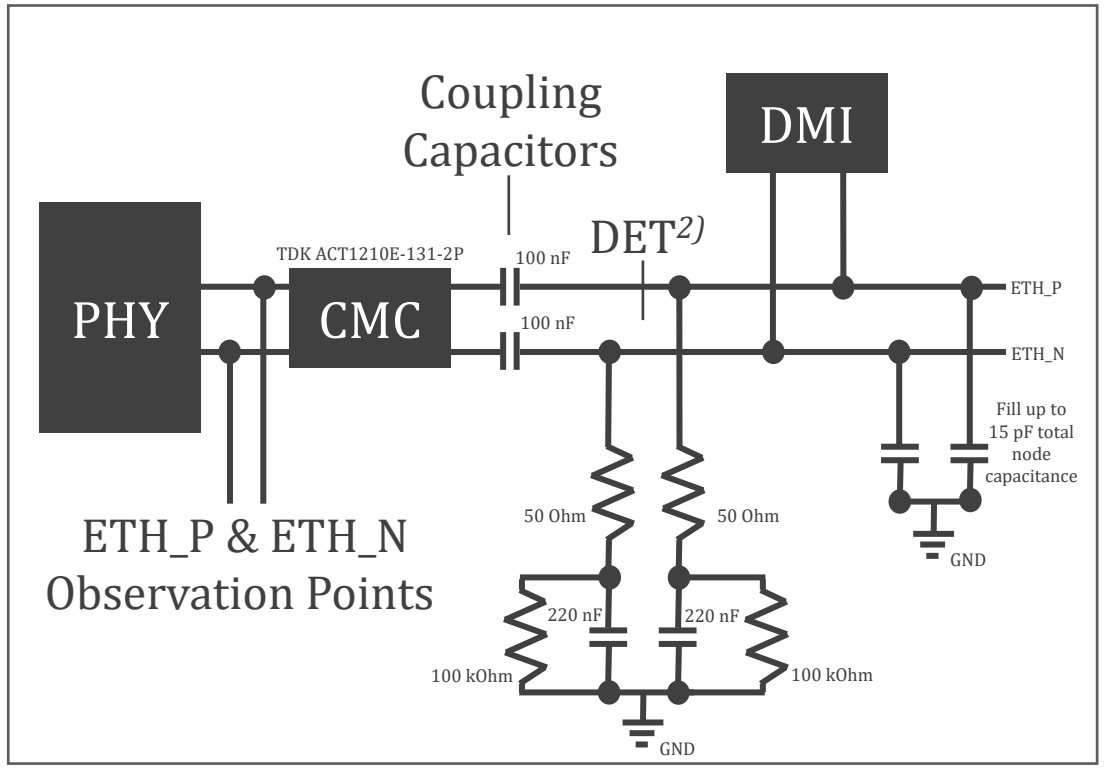
Point of investigation

- Goal: analyze the impact of MPoE on the signal integrity
- Variants used in simulation
  - Two different in-vehicle network topology designs
  - Supply voltage of the PSE: 12V, 24V and 48V
  - Corner cases of the PHY and transmission line incl. tolerances and temperature
  - Gaussian noise injection with 200 mV peak-to-peak
    Hint: The simulation was still running after the submission deadline for this presentation. If you are interested in the results, please contact p.isensee@cs-group.de
- Not part of the current investigation
  - Charging transients that occur during the system's ramp-up phase
  - The impact of voltage regulators in PSE and PDs, and the related switching noise

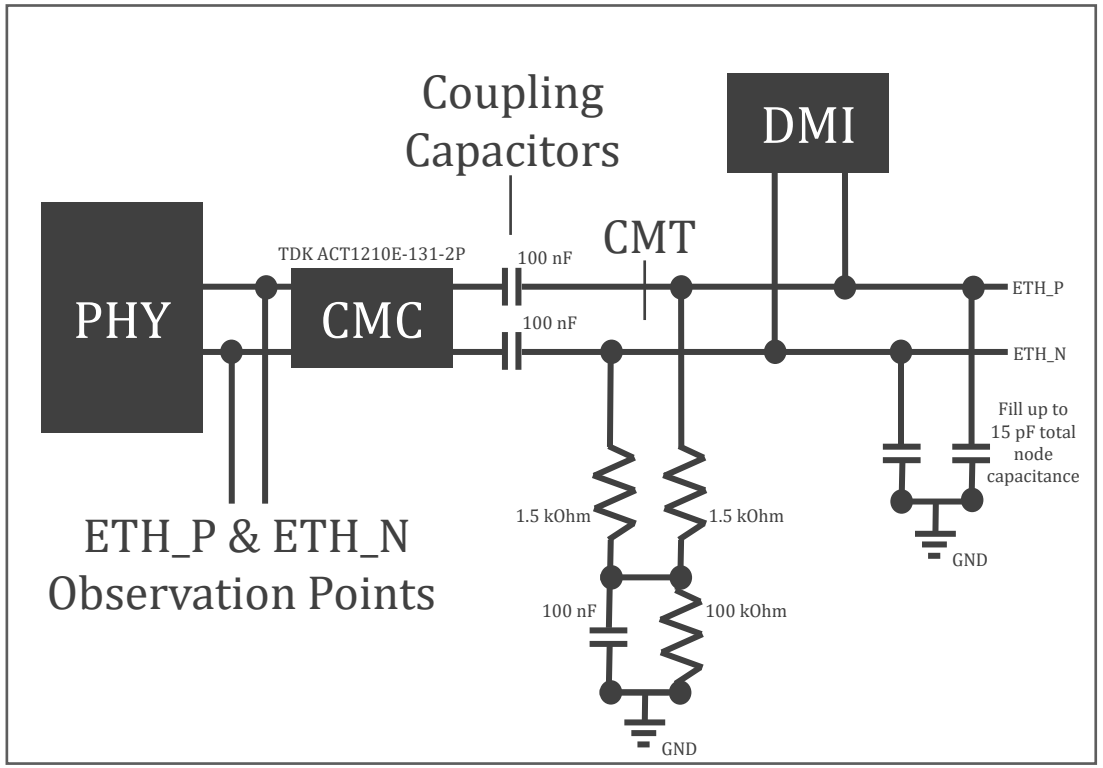
10BASE-T1S In-Vehicle Network Validation

Simulation setup – ECU circuitry

- End node[1)] as PSE



- Drop node as PD



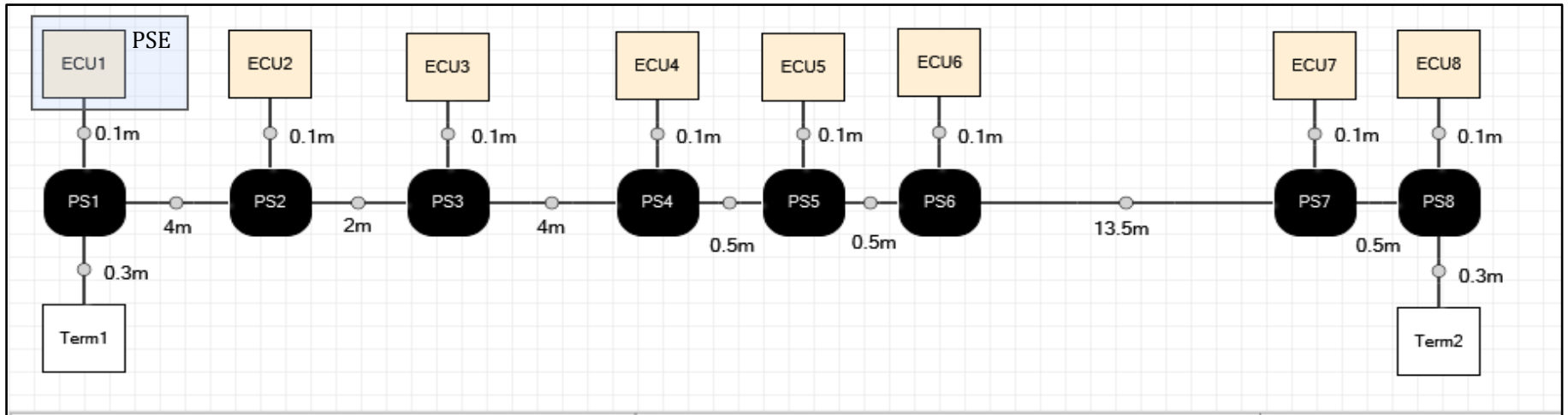
[1)] The second end node is set up as PD and only include the DET (Differential End Termination) in topology 2.

[2)] DET changed as stated in Microchips "LAN86xx-Using-Power-over-Data-Line-in-10BASE-T1S-Application-Note-6"

10BASE-T1S In-Vehicle Network Validation

Simulation setup – In-vehicle network topology design

- Simple topology like defined in OPEN Alliance system implementation
  - Power Sourcing Equipment (PSE) = ECU1; remaining ECUs = PD (Powered Device)
  - A UTP cable model of type FLR9Y 2*0,35 QMM-SN SL13 is used for all connections



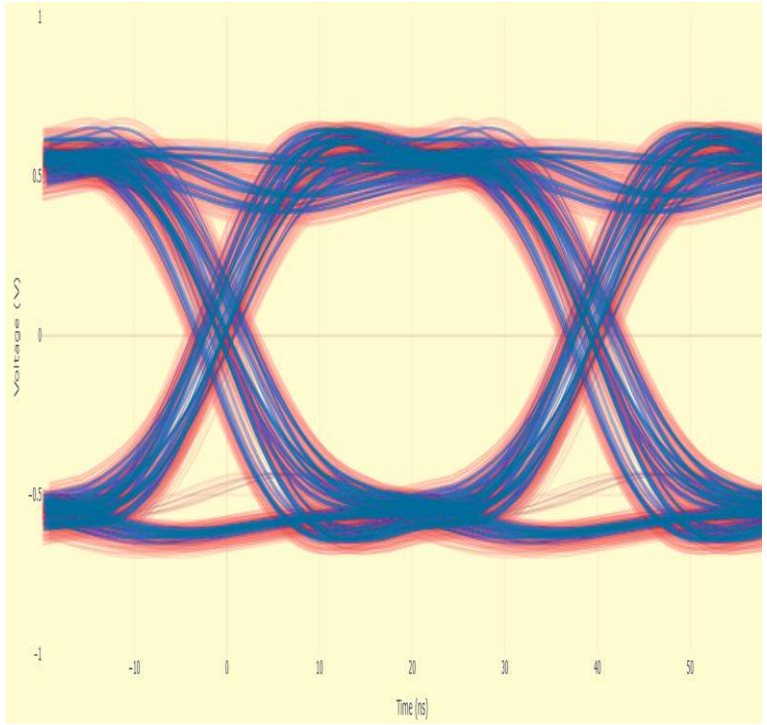
General Information				Further Information				Legend	
Number of ECUs:	8	Number of Passive Stars:	8	Total Length:	26.400 m	Max. Number of nodes on a splice:	2		DROP_Node
Longest terminated stub/node:	0.300 m (Term1, Term2)	Shortest distance of two non-terminated stubs/nodes:	0.700 m	Shortest non terminated stub/node	0.100 m (ECU1, ECU2, ECU3, ECU4, ECU5, ECU6, ECU..)	Distance of terminated stubs/nodes:	25.600 m		PassiveStar
Shortest terminated stub/node:	0.300 m (Term1, Term2)	Shortest distance of two Passive Stars:	0.500 m	Longest non terminated stub/node:	0.100 m (ECU1, ECU2, ECU3, ECU4, ECU5, ECU6, ECU..)	Longest distance of two non-terminated stubs/nodes:	25.200 m		Termination

10BASE-T1S In-Vehicle Network Validation

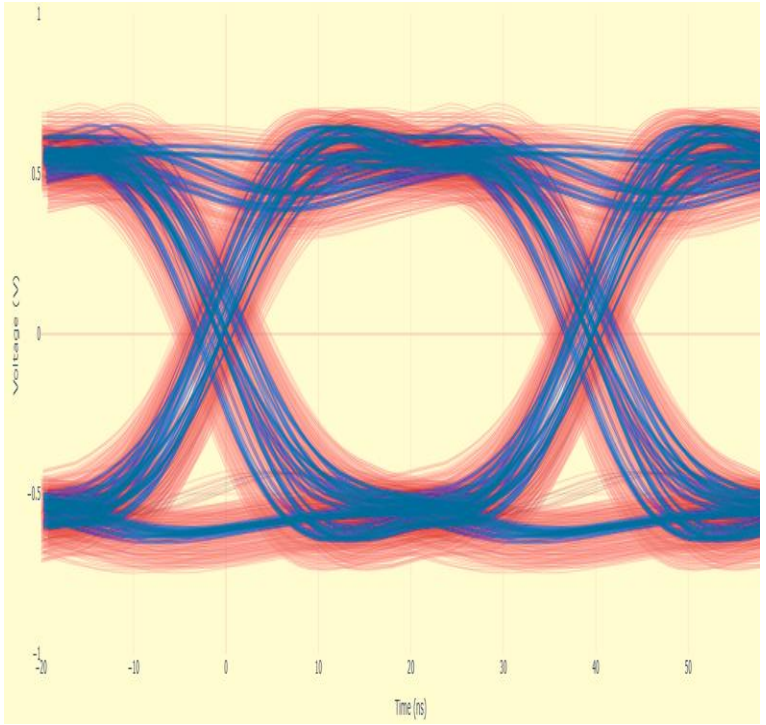
Simulation outcome

Note: All eye diagrams include typical conditions and corner cases of the PHY and the transmission line.

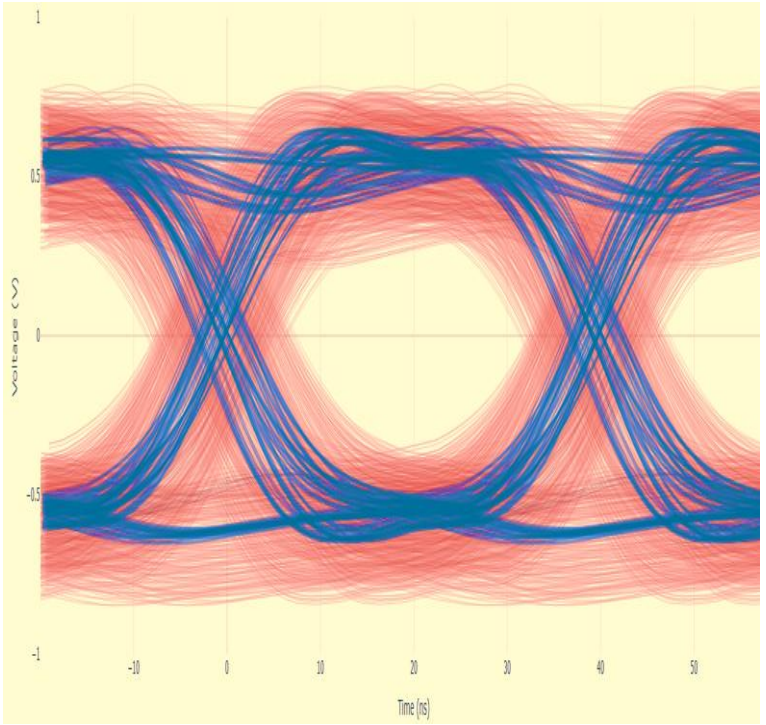
12V: Jitter RMS=0.8ns | P2P=3.3ns



24V: Jitter RMS=1.4ns | P2P=4.2ns



48V: Jitter RMS=2.9ns | P2P=6.7ns

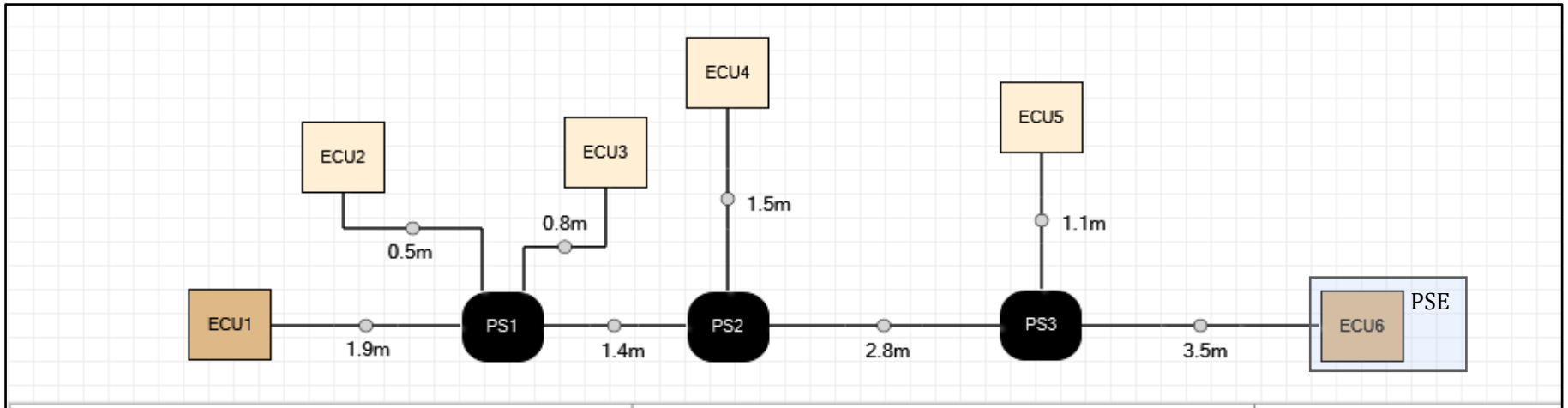


BLUE: reference signal without PoDL (Jitter RMS=0.6ns | P2P=2.9ns); **RED**: with PoDL

10BASE-T1S In-Vehicle Network Validation

Simulation setup – In-vehicle network topology design

- Complex topology outside the IEEE boundaries (based on real OEM studies)
  - Power Sourcing Equipment (PSE) = ECU6; remaining ECUs = PD (Powered Device)
  - A UTP cable model of type FLR9Y 2*0,35 QMM-SN SL13 is used for all connections



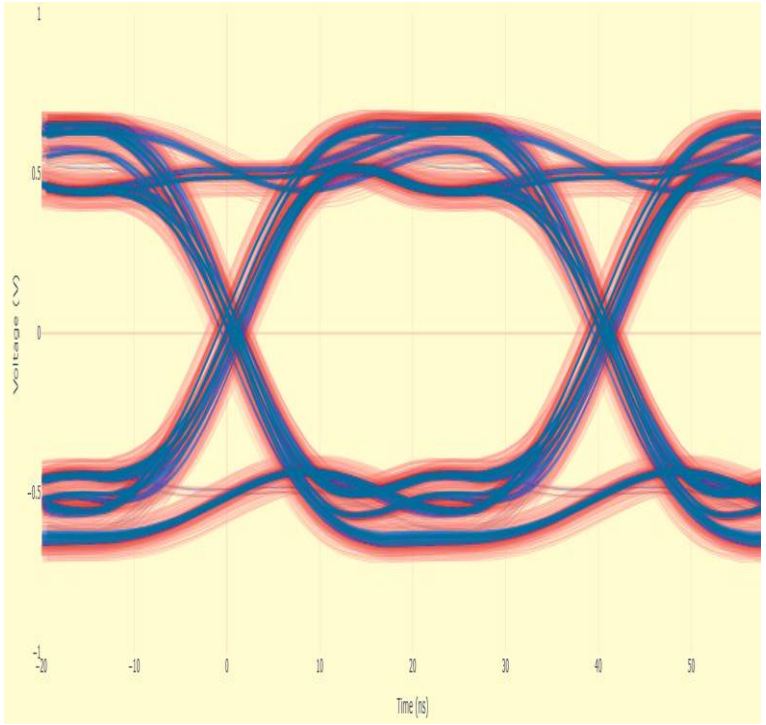
General Information				Further Information				Legend	
Number of ECUs:	6	Number of Passive Stars:	3	Total Length:	13.500 m	Max. Number of nodes on a splice:	3		END_Node
Longest terminated stub/node:	3.500 m (ECU6)	Shortest distance of two non-terminated stubs/nodes:	1.300 m	Shortest non terminated stub/node	0.500 m (ECU2)	Distance of terminated stubs/nodes:	9.600 m		DROP_Node
Shortest terminated stub/node:	1.900 m (ECU1)	Shortest distance of two Passive Stars:	1.400 m	Longest non terminated stub/node:	1.500 m (ECU4)	Longest distance of two non-terminated stubs/nodes:	6.100 m		PassiveStar

10BASE-T1S In-Vehicle Network Validation

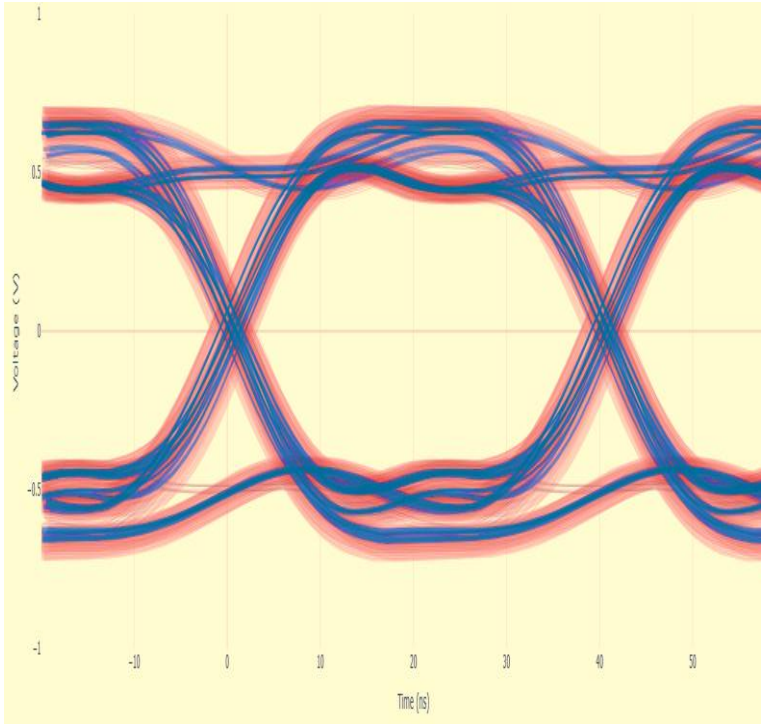
Simulation outcome

Note: All eye diagrams include typical conditions and corner cases of the PHY and the transmission line.

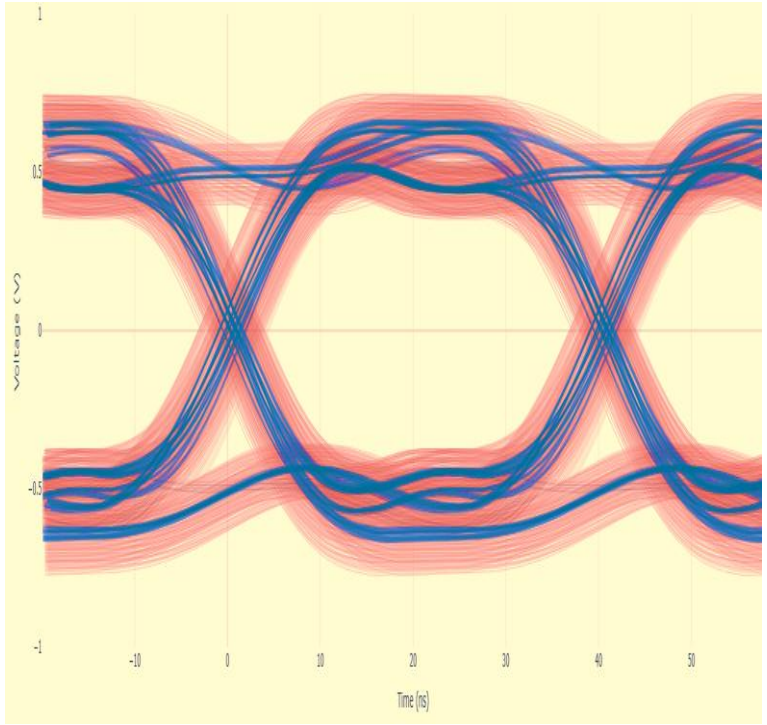
12V: Jitter RMS=1.8ns | P2P=3.4ns



24V: Jitter RMS=2.0ns | P2P=3.6ns



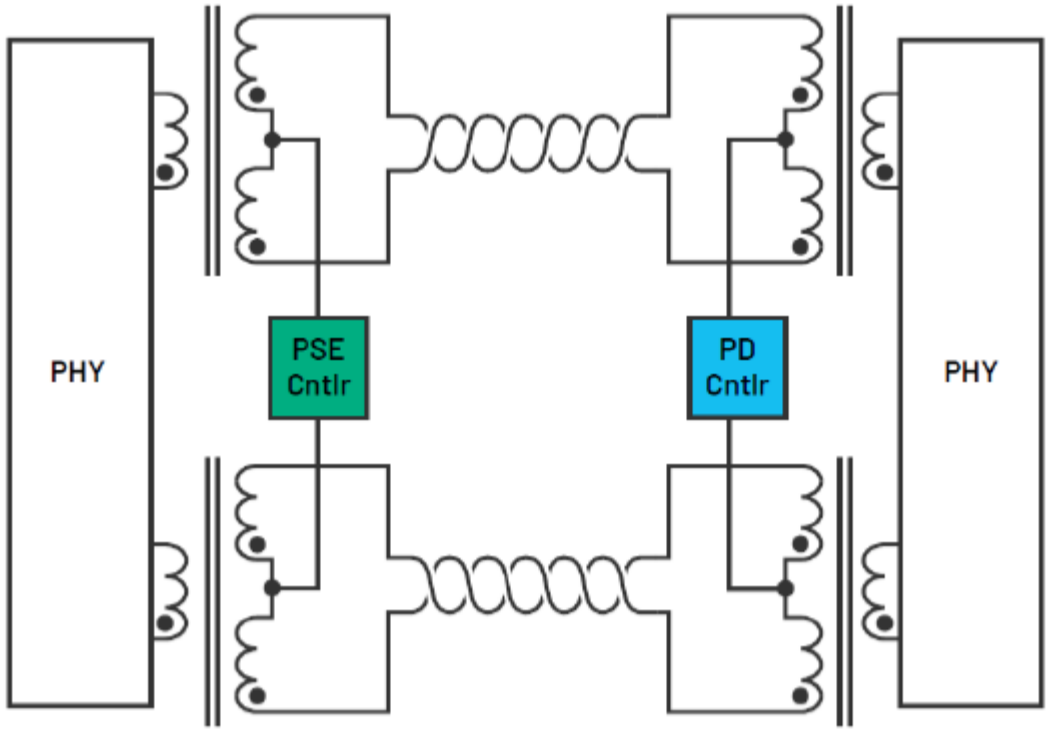
48V: Jitter RMS=2.6ns | P2P=4.6ns



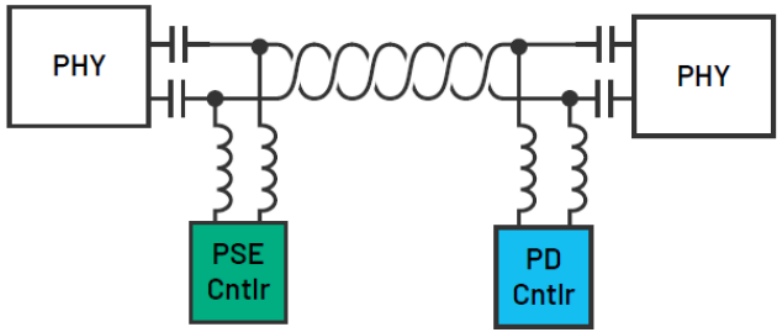
BLUE: reference signal without PoDL (Jitter RMS=1.4ns | P2P=2.4ns); **RED**: with PoDL

10BASE-T1S In-Vehicle Network Validation

PoE vs. PoDL - Trafo to capacitors



- 2-Pair or 4-Pair Ethernet + Power PoE



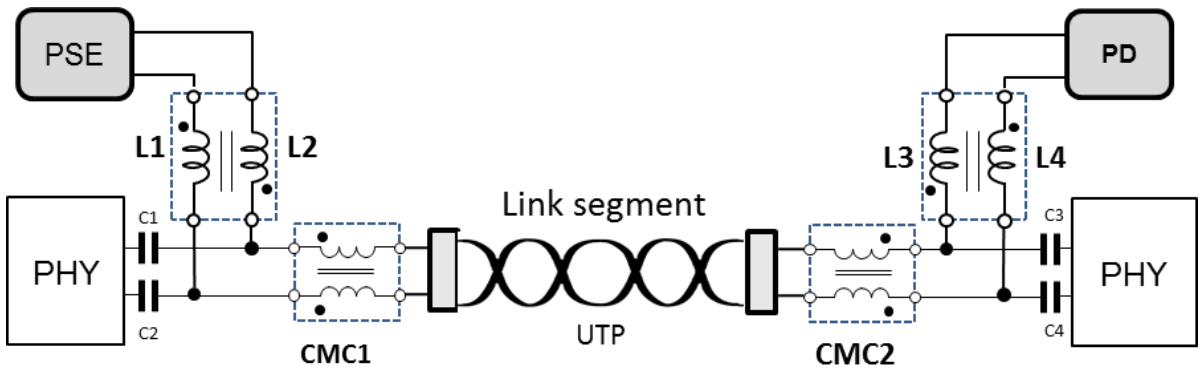
- Single-Pair Ethernet + Power
  - PoDL – Power over Data Lines
  - SPoE – Single-Pair Power over Ethernet
  - MPoE – Multidrop Power over Ethernet

Ref.: Michael Paul, ADI, AEC2025, T1M Power MPoE Overview

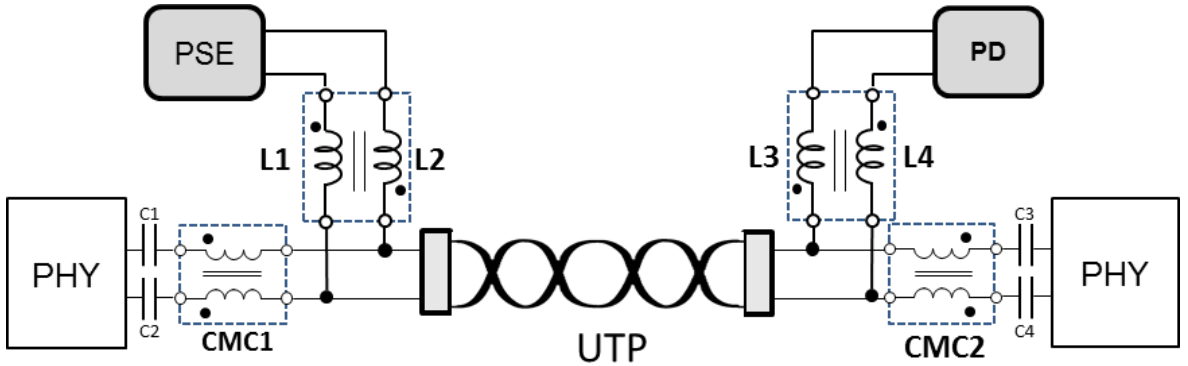
10BASE-T1S In-Vehicle Network Validation

PoDL Circuit Implementation

- LINE-Side vs PHY-Side Power Injection



- „standard“ PoDL circuit implementation for LINE-Side injection



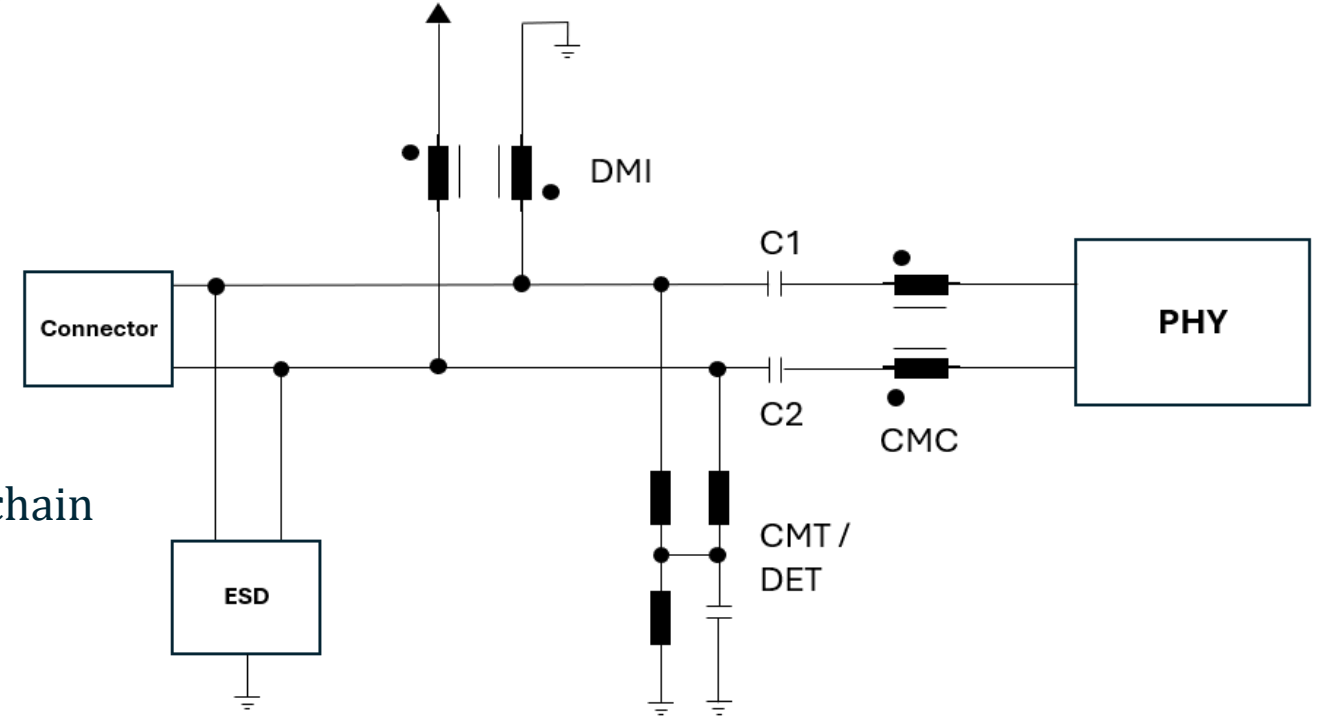
- proposed PoDL circuit implementation, **PHY-Side injection**

Ref.: Felipe Jerez, TDK, ICSJ2019 (Kyoto, Japan), Inductors for modern Power over Signal applications in automotive

10BASE-T1S In-Vehicle Network Validation

PoDL implementation challenges

- PoDL Inductors
  - Case size
  - Rated current
  - ACQ-200, temperature stability
  - 2 x Single Inductors vs DMI
  - Multidrop vs point to point vs Daisy chain
  - Right Impedance (RL and MC limits)

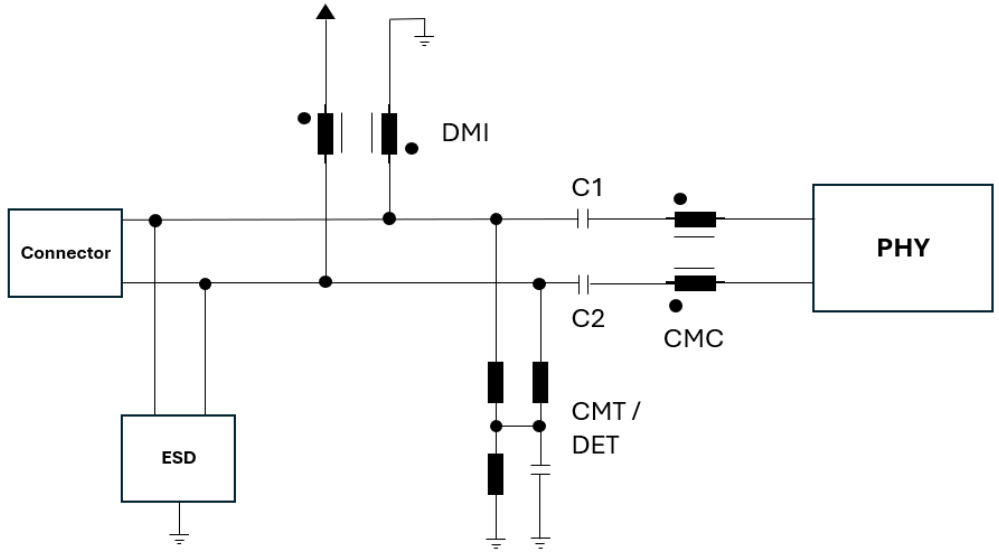


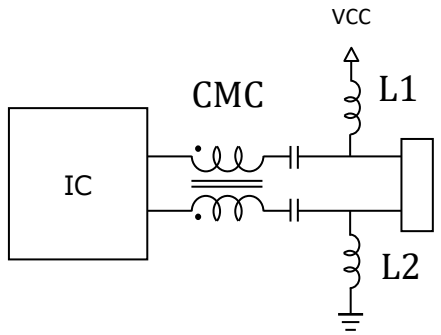
Ref.: Abdelkader Hessainia, Ampere, AEC2025, 10BASE-T1S Ethernet New technology new challenges

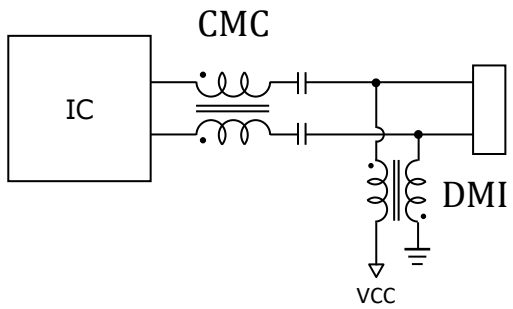
10BASE-T1S In-Vehicle Network Validation

PoDL challenges – 2x Single Inductor vs DMC /DMI

2 x Single Inductor	DMI
Low stray capacitance	low stray capacitance is visible with the right design
Low tolerance for good mode conversion performance is needed	Good mode conversion performance
Low surface area	A 32 case size (3.2x2.5x2.5) components is visible







Ref.: Jibu Palathanam, Yu-Ting Wu, Ford, IEEE ETH TechDay2024, Node Count Analysis in 10Base-T1S Ethernet

Ref.: Abdelkader Hessainia, Ampere, AEC2025, 10BASE-T1S Ethernet New technology new challenges

10BASE-T1S In-Vehicle Network Validation

Right Impedance for 10BASE-T1S

The IEEE802.3cg™ Physical Layer specification is showing the minimum needed MDI impedance at 80µH (IEEE802.3cg™ 147.9.2 MDI electrical specification). The minimum L_{PoDL} (series Inductance) values are calculated out of the transmitter output voltage and transmitter output droop according to the different physical layer specifications. For 10BASE-T1S it´s a droop time of 800nsec, phy resistance of 100Ω, droop time of 800 nsec and a voltage droop of 30% for the differential manchester encoding signal. This leads to a LPoDL of 112µH taking coupling and tolerance of the DMI into account. This value can be achieved with the right DMI and leads to a single inductance of 36µH and a PoDL Inductance of (LPoDL) of ~110µH tacking the tolerance and coupling factor into account.

$$L(H) \geq \frac{-RPHY * t_{Droop}}{ln\left(1 - \frac{U_{Droop}}{U_{peak}}\right)}$$

Electrical parameter	DMI for 10BASE-T1S	Single Inductor
Data rate	10Mbps	10Mbps
Inductance [µH]	**2x36**	**67**
C_{stray} [pF]	<=5	<=5
MC (delt L)	<=5%	<=5%
LPoDL [µH] series Inductance for DMI, Single Inductance L [µH]	>80, ~**110**	**>80, ~67**

Parameter	10BASE-T1S
Transmitter output voltage [V], U_{peak}	1.0
Droop Value (30%) [V], U_{Droop}	0.3
PHY resistance [Ohm] R_{PHY}	100
Droop time [nsec], t_{Droop}	800
Loop Inductance [µH], L_{PoDL}	112
Worst case V_{pp_max}	1.2V
Best case V_{pp}	0.8V
Typical case V_{pp}	1.0V

Ref.: IEEE 802.3cg, PL Specification and Management Parameters for 10 Mb/s Operation and Associatied Power Delivery over a Single Balanced Pair of Conductors

10BASE-T1S In-Vehicle Network Validation

Right stray capacitance for 10BASE-T1S DMIs

The Open Alliance IEEE 10BASE-T1S Implementation Specification at the TC14 – System Implementation defines the $\mathbf{C_{MDI}}$ **<= 25pF** including 10pF for the PHY, 10pF for the CMC and 5pF rest including DMI, tracing (1pF / inch) and connectors.

Electrical paramter	DMI for 10BASE-T1S
Data rate	10Mbps
Inductance [µH]	2x36
Cstray [pF]	**<=5**
MC (delt L)	<=5%
LPoDL [µH] series Inductance for DMI	>80, ~110

Ref.: Open Alliance, TC14, IEEE 10BASE-T1S Implementation Specification, version 1.0, 15 February 2023

10BASE-T1S In-Vehicle Network Validation

PoDL Power Classes

According to the power classes described in IEEE Std 802.3bu™ and 802.3cg™ a complete set of inductors must be developed to achieve the requirements in terms of power, voltage and current.

	12 V unregulated PSE		12 V regulated PSE		24 V unregulated PSE		24 V regulated PSE		48 V regulated PSE	
Class	0	1	2	3	4	5	6	7	8	9
$V_{PSE(max)}$ (V)[a]	18	18	18	18	36	36	36	36	60	60
$V_{PSE\_OC(min)}$ (V)[b]	6	6	14.4	14.4	12	12	26	26	48	48
$V_{PSE(min)}$ (V)	5.6	5.77	14.4	14.4	11.7	11.7	26	26	48	48
$I_{PI(max)}$ (mA)[c]	101	227	249	471	97	339	215	461	735	1 360
$P_{Class(min)}$ (W)[d]	0.566	1.31	3.59	6.79	1.14	3.97	5.59	12	35.3	65.3
$V_{PD(min)}$ (V)	4.94	4.41	12	10.6	10.3	8.86	23.3	21.7	40.8	36.7
$P_{PD(max)}$ (W)[e]	0.5	1	3	5	1	3	5	10	30	50

- Power classes according to 802.3bu™

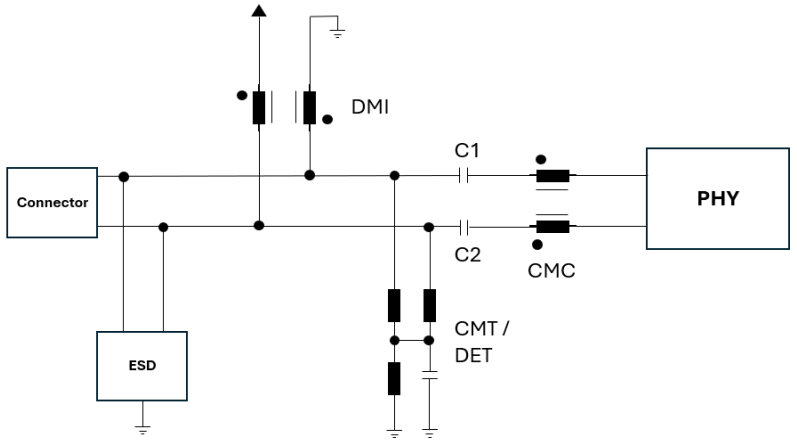
Class	10	11	12	13	14	15
$V_{PSE(max)}$ (V)	30	30	30	58	58	58
$V_{PSE\_OC(min)}$ (V)	20	20	20	50	50	50
$V_{PSE(min)}$ (V)	20	20	20	50	50	50
$I_{PI(max)}$(mA)	92	240	632	231	600	1579
$P_{class(min)}$ (W)	1.85	4.8	12.63	11.54	30	79
$V_{PD(min)}$ (V)	14	14	14	35	35	35
$P_{PD(max)}$ (W)	1.23	3.2	8.4	7.7	20	52

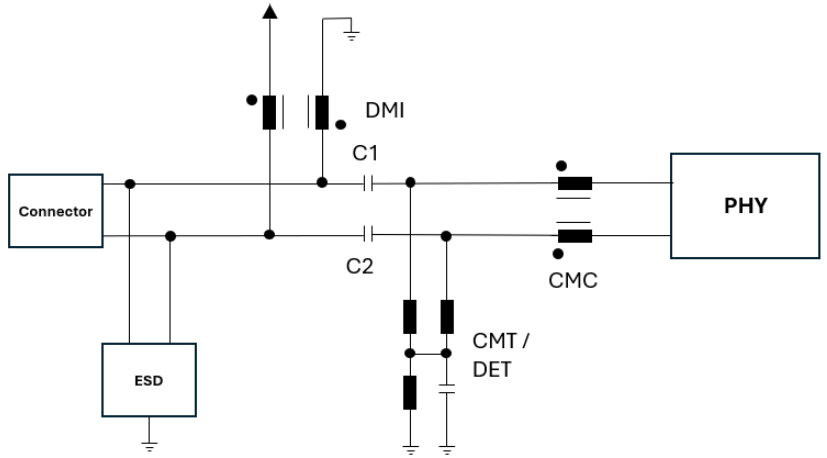
- Power classes according to 802.3cg™

10BASE-T1S In-Vehicle Network Validation

PoDL in multidrop topology like 10BASE-T1S

Below the CMT / DET Termination is put before the capacitors. Some implementations also show the termination behind the capacitors





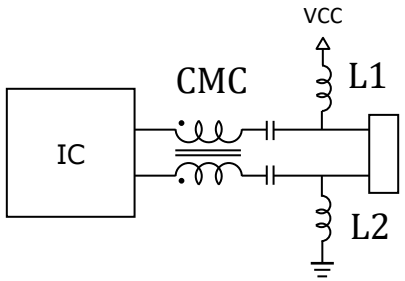
The system can be implemented with a comma mode choke (CMC) and a comma mode termination (CMT) as it is recommended in the Open Alliance “10BASE-T1S System Implementation Specification”. To introduce some differential signal filtering a differential mode inductor so called DMI is needed. Since the immunity strongly depends on the shielding of the cable it´s recommended to use a CMC in the UTP case. To not oversize and discriminate the performance of the CMC the LINE-Side injection should be piked. So, it is guaranteed that the high current is flowing via the DMI and not the CMC. To reduce the capacitance of the system different CMC are available and DMI with low capacitance.

10BASE-T1S In-Vehicle Network Validation

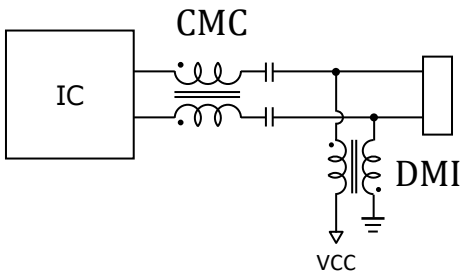
Measurement: single Inductor vs DMI

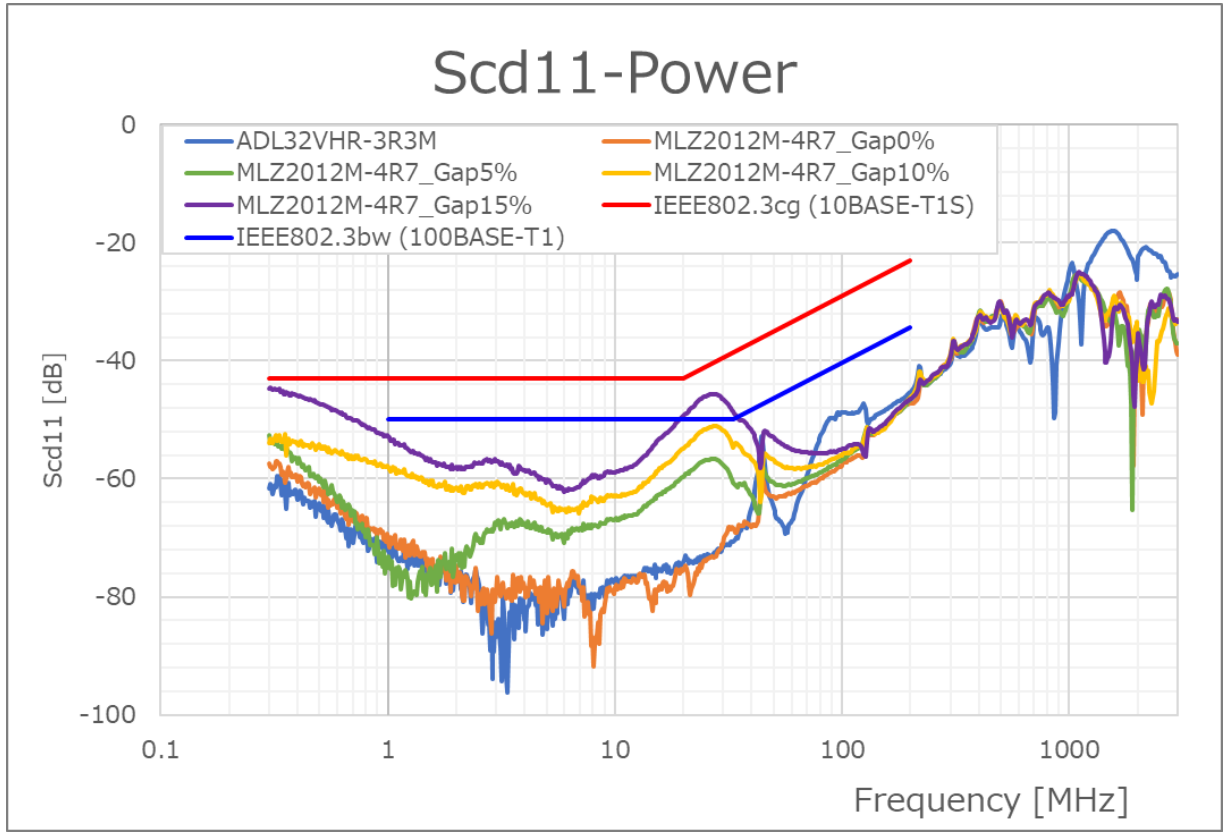
Mode Conversion (Scd11) of a single Inductor (MLZ) and a DMI (ADL32VHR) compared to the 10BASE-T1S and 100BASE-T1 limit

2 x Single Inductor



DMI





Conclusion:
Delta L (difference L1, L2): minimum of 5% tolerance is needed to guarantee the 10BASE-T1S, 100BASE-T1 limits

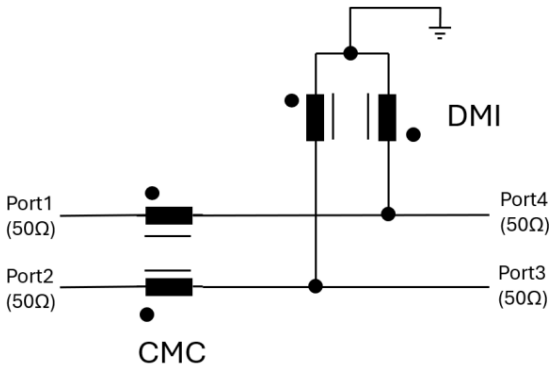
The percentage is describing the tolerance from the single component Inductor. Gap5% means 5% tolerance between L1 and L2

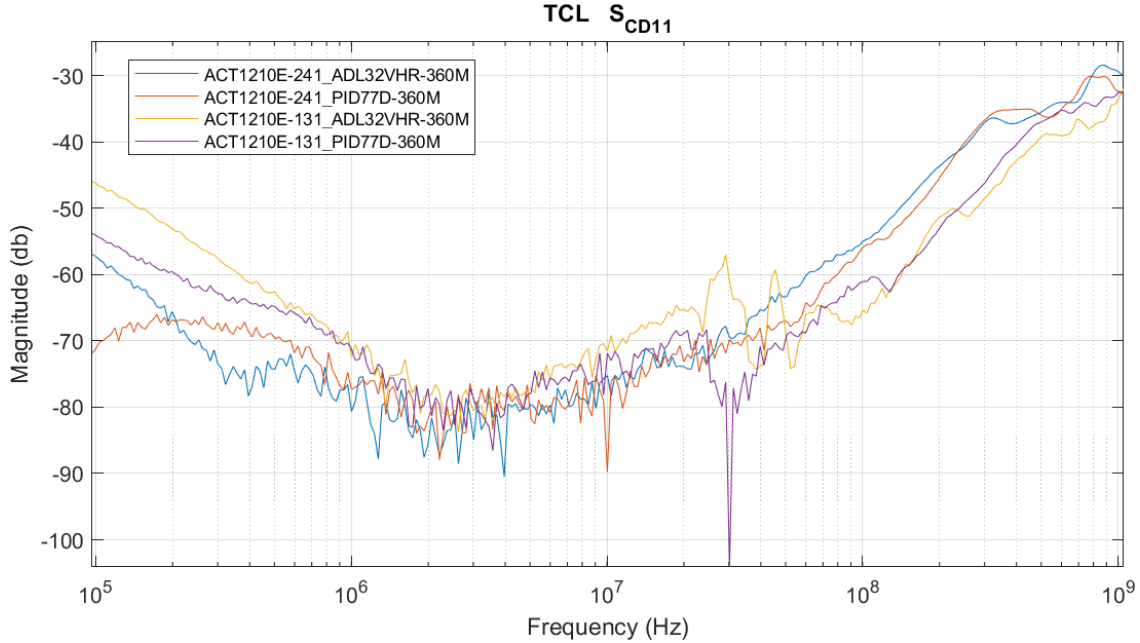
10BASE-T1S In-Vehicle Network Validation

Measurement: Mode conversion

To reduce the complexity of the measurement setup only a combination of the CMC/DMI can be measured to characterize the inductors. The DMI is put to ground (GND) on one side, and the 4-Port S-Parameters are measured.

CMC: ACT1210E-131/241
DMI: ADL32VHR-360M, PID77D-360M





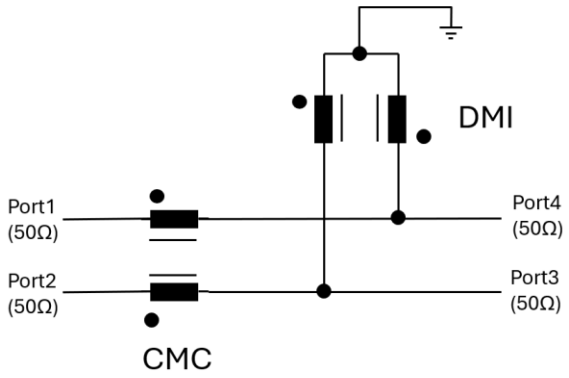
As L1 and L2 are implemented as a Differential Mode Inductor (DMI) by using the same magnetic core which results into a better Mode Conversion performance (Scd22, Scd12, Scd21, Sdc12 and Scd21) in comparison with two single coils.

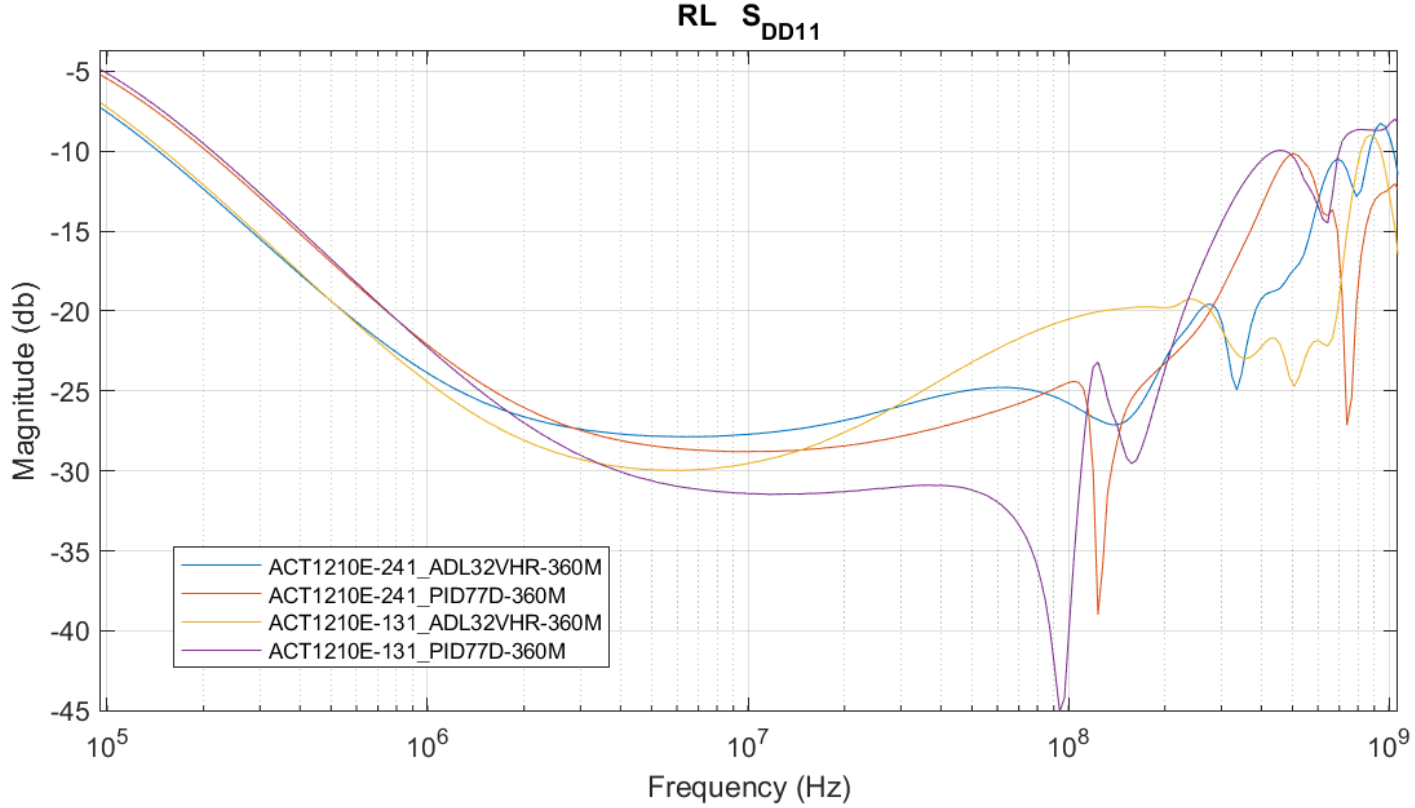
10BASE-T1S In-Vehicle Network Validation

Measurement: Return loss

Improvements in RL → smaller case size and higher current
Return Losses of a PoDL circuit (DMI+CMC)

CMC: ACT1210E-131/241
DMI: ADL32VHR-360M, PID77D-360M





10BASE-T1S In-Vehicle Network Validation

Measurement

CMC	PoDL inductors				
	Component	*Inductance [µH]*	*Idc [mA]*	*Cstray [pF]*	*Size [mm]*
CMC, (ACT1210E-241, ACT1210E-131)	DMI, (ADL32VHR-360M)	2x36	270	1.0	3.2x2.5x2.5
	DMI, (ADM45FDR-360M)		330	2.2	4.5x3.2x3
	DMI, (PID77D-360M)		690	2.5	7x7x7
	DMI, (PID120HD-360M)		1900	4.0	12x12x10.5
	DMI, (PID150HD-360M)		2600	4.5	15x15x14.5

- Improvements in C_{stray} → more drop nodes are feasible and different cable length between the nodes
- For the DMI the C_{stray} sould stay below 5pF

10BASE-T1S In-Vehicle Network Validation

Conclusion

A set of different DMIs is needed for the power classes and different CMCs are visible depending on the number of nodes.

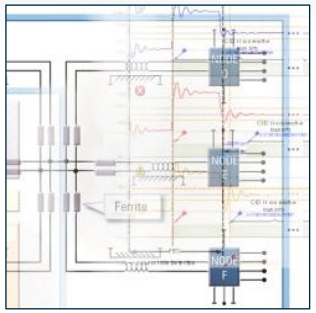
CMC	PoDL inductors						
	Component	*Inductance [µH]*	*Idc [mA]*	*RDC [Ohms]*	*Cstray [pF]*	*Size [mm]*	*Rated voltage V_R [V]*
CMC, (ACT1210E-241, ACT1210E-131)	DMI, (ADL32VHR-360M)	2x36	270	1.7	1.0	3.2x2.5x2.5	12, 24, 48
	DMI, (ADM45FDR-360M)		330	1.1	2.2	4.5x3.2x3	12
	DMI, (PID77D-360M)		690	0.25	2.5	7x7x7	12, 24, 48
	DMI, (PID120HD-360M)		1900	0.066	4.0	12x12x10.5	12, 24, 48
	DMI, (PID150HD-360M)		2600	0.032	4.5	15x15x14.5	12, 24, 48

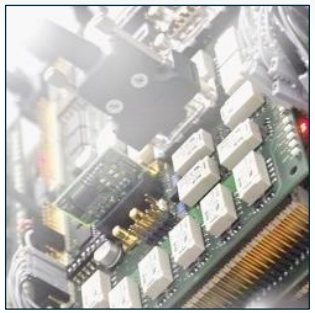
10BASE-T1S In-Vehicle Network Validation

Conclusion

On the one hand, 10BASE-T1S means a **flexible** and **efficient,**
as well as a **cost reduced usage**, on the other hand, **complex topologies** and
additional **functionalities like MPoE** result in an
advanced approval process of the physical layer.

- Simulation is a very effective tool by the usage of automation and an excellent approach to overcome design problems at early stage of IVN development or upgrades of existent designs
- The general analysis includes tolerances of components, temperature conditions and deviations from the standard. If necessary, this is supplemented by a single verification measurement
- PoDL does impact signal integrity in 10BASE-T1S multidrop systems, so it should be included a validation step, particularly for extended topologies
- Next Steps
  - Further standardization work is necessary to establish PoDL in a 10BASE-T1S multidrop system
  - Deep physical layer analysis of node compensation with TCIs (Trunk Component Inductors)





Thanks for your attention!

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