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Enabling Time-Aware Shaper on Half-Duplex Ethernet PLCA Multidrop

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Agenda

- Introduction
- Time-Aware Shaper (TAS)
- 10BASE-T1S
  - Physical Layer Collision Avoidance (PLCA)
- TAS + PLCA
- Full-duplex switched Ethernet *vs* Half-duplex PLCA Multidrop Ethernet
  - Results
- Conclusion
  - Future work

Introduction

Most Ethernet implementations today

- Switched networks with full-duplex links

Problems

- They may be costly for some use cases, mainly automotive
- Over 90% of the current internal communication links need less than 10 Mbps[1]
- 100BASE-T1 is not cost-efficient for replacing CAN (Controller Area Network) or CAN-FD (CAN with Flexible Data Rate)

Solution

- 10BASE-T1S

Time-Sensitive Networking (TSN)

- Time Synchronization, Ultra reliability, Bounded low latency, and Dedicated Resources & API

TSN includes IEEE 802.3Qbv

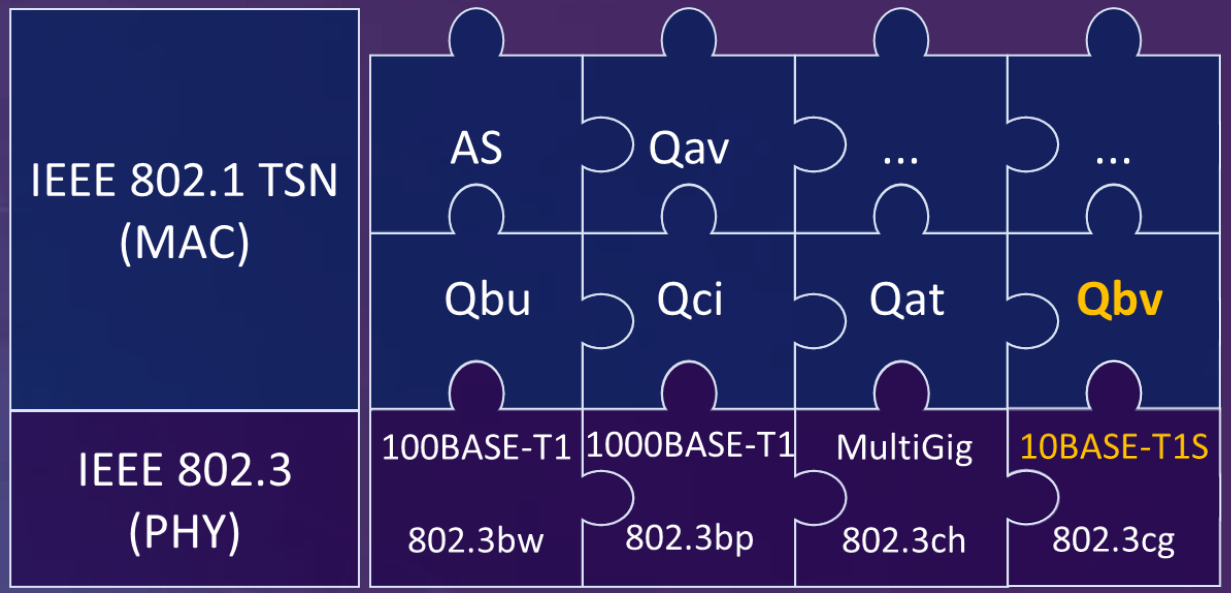
- Time-Aware Shaper (TAS)
- Ultra-low latency, jitter, and loss
- TAS is a solution for deterministic systems
  - Real-time and safety-critical applications

[1] K. Matheus and T. Königseder, Automotive Ethernet, 3rd ed. Cambridge University Press, 2021.

Introduction

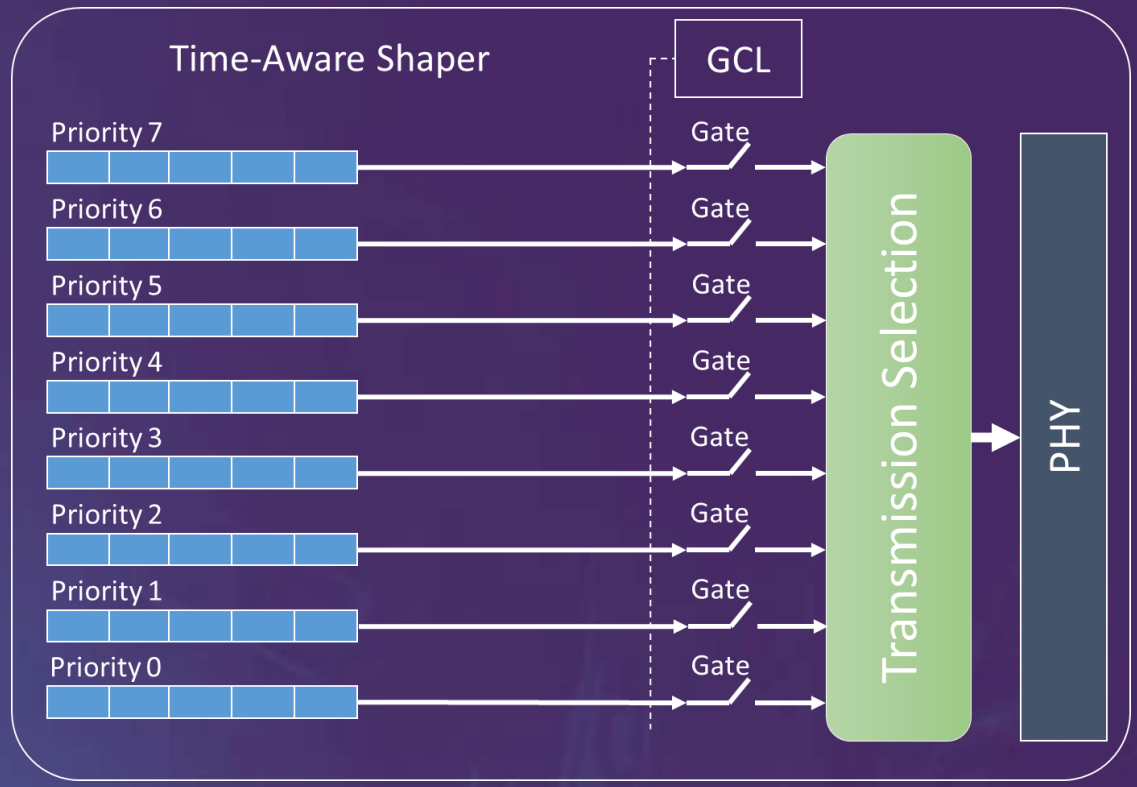
The integration of TAS and 10BASE-T1S PLCA enables many possibilities

- No gateways
- End-to-end transmissions of scheduled traffic Ethernet flows
- All-Ethernet Vehicle



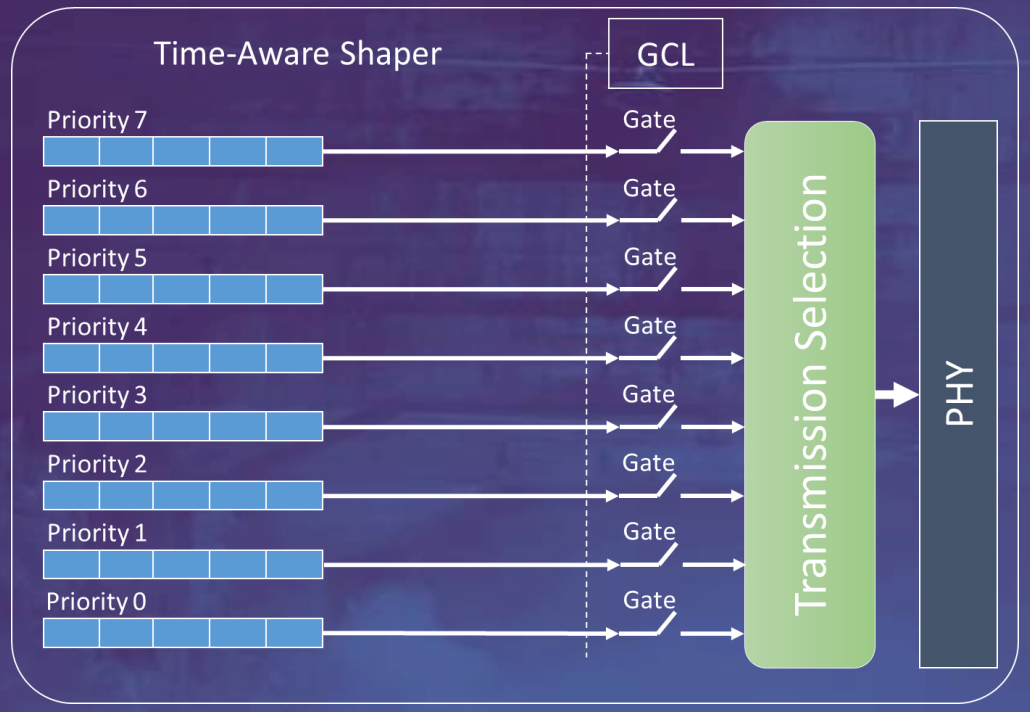
Time-Aware Shaper

- Gate Control List (GCL)
  - Clock-based open-close gate scheduling for all priority queues
- Scheduled Traffic (ST)
- Time slots for transmissions (windows)
  - Exclusive windows
    - Lowest delay bounds
    - More complex to provide (NP-hard)
    - Similar to Time Division Multiple Access (TDMA)
    - Desired in automotive
  - Overlapping windows
    - Low delay bounds
    - More simple to provide
    - Strict Priority (no preemption)
    - Not desired in automotive



Time-Aware Shaper

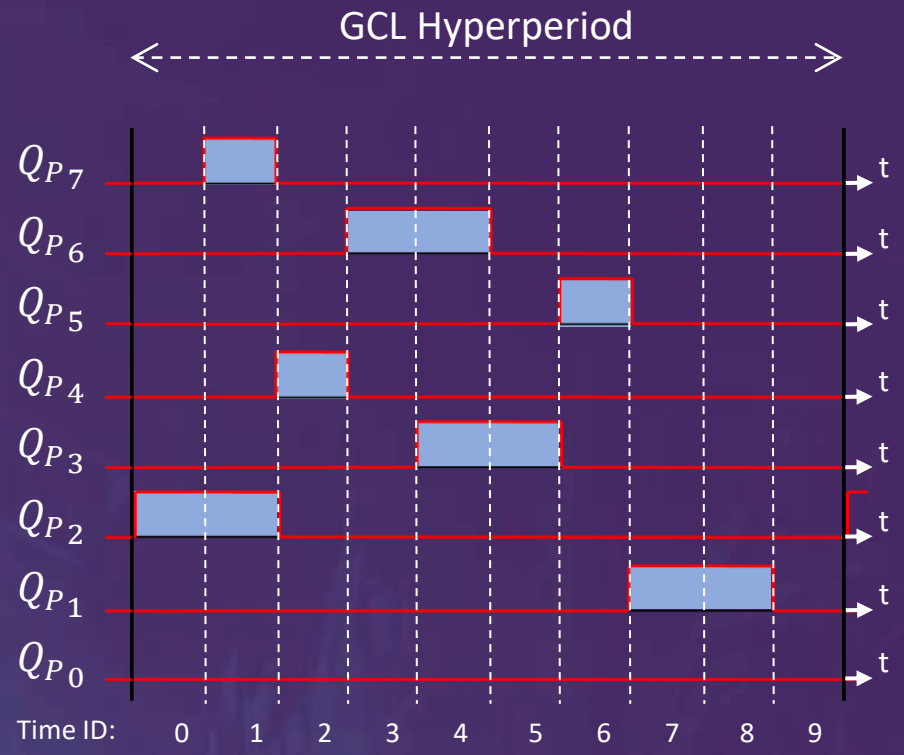
Ethernet interface



GCL scheduling

Gate Control List (GCL)	
Time ID	**Gate States**
0	00000100
1	10000100
2	00010000
3	01000000
4	01001000
5	00001000
6	00100000
7	00000010
8	00000010
9	00000000

Gate states over time



Time-Aware Shaper

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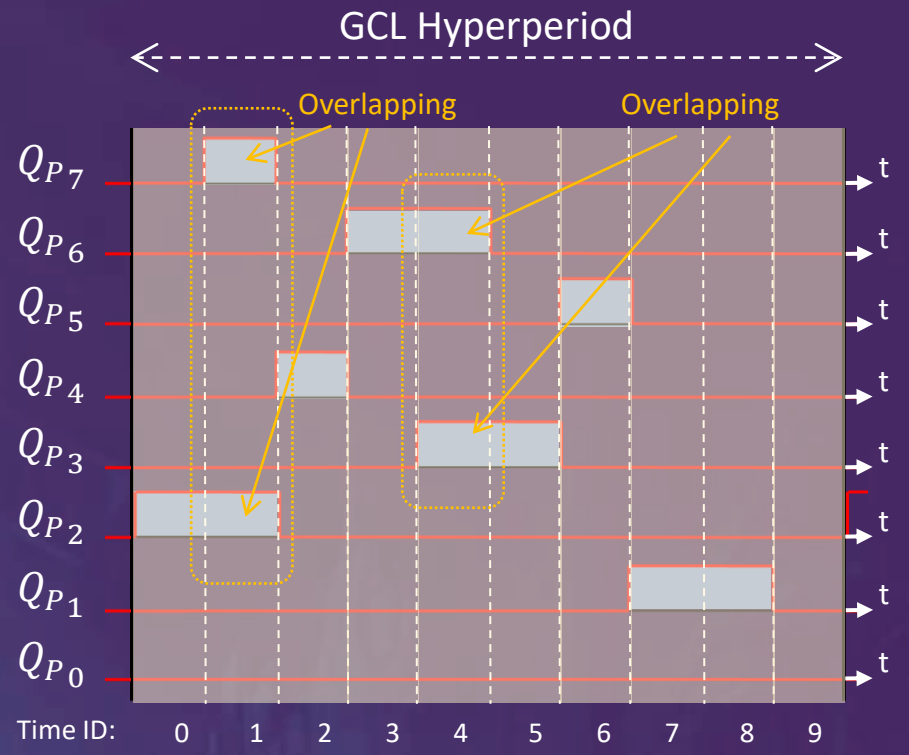
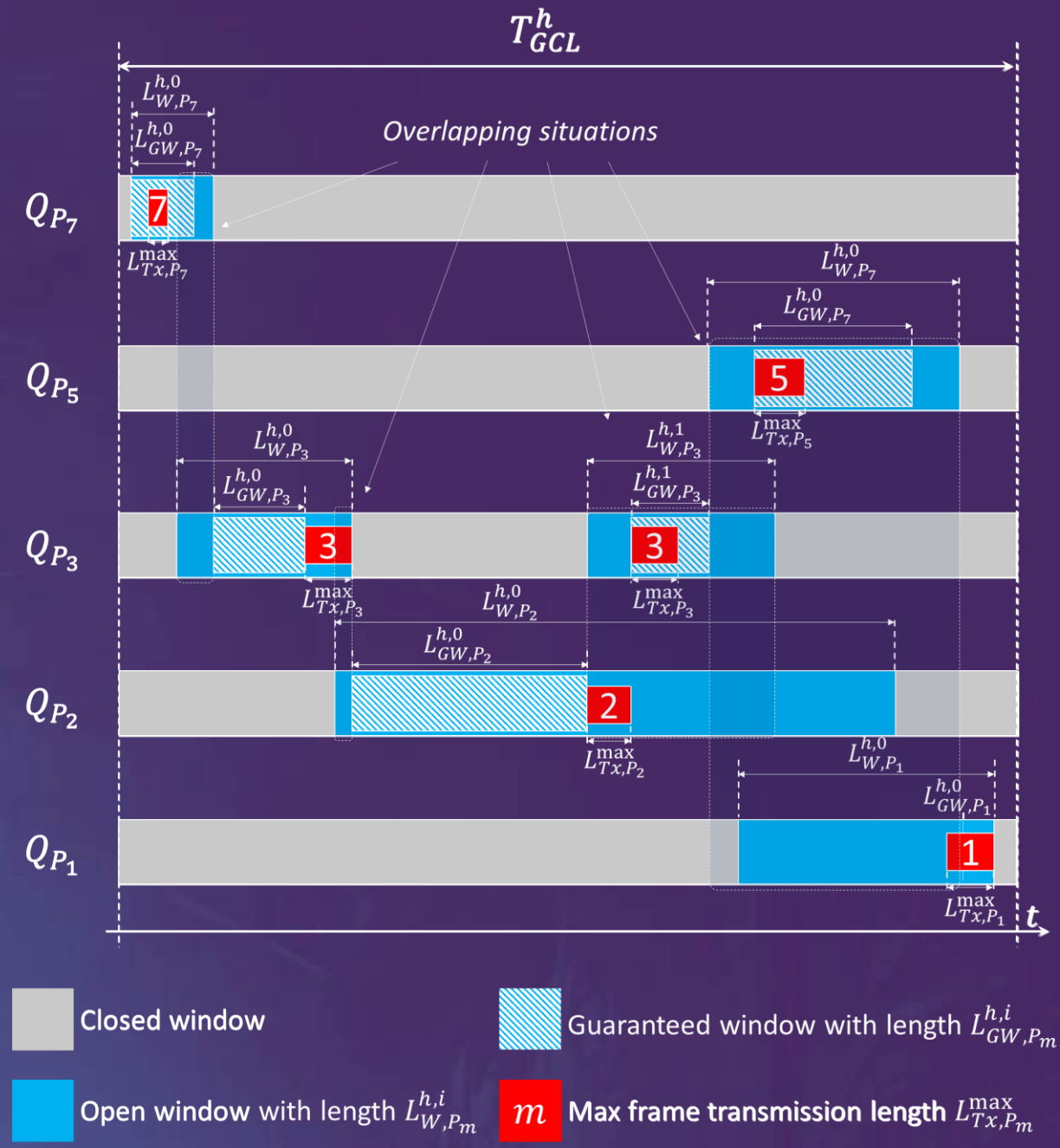


Time-Aware Shaper

- Transmissions within the open window
- The guard band is considered
- Overlapping among windows
  - In the worst case, the whole window is not available
  - Guaranteed windows must be calculated[2]

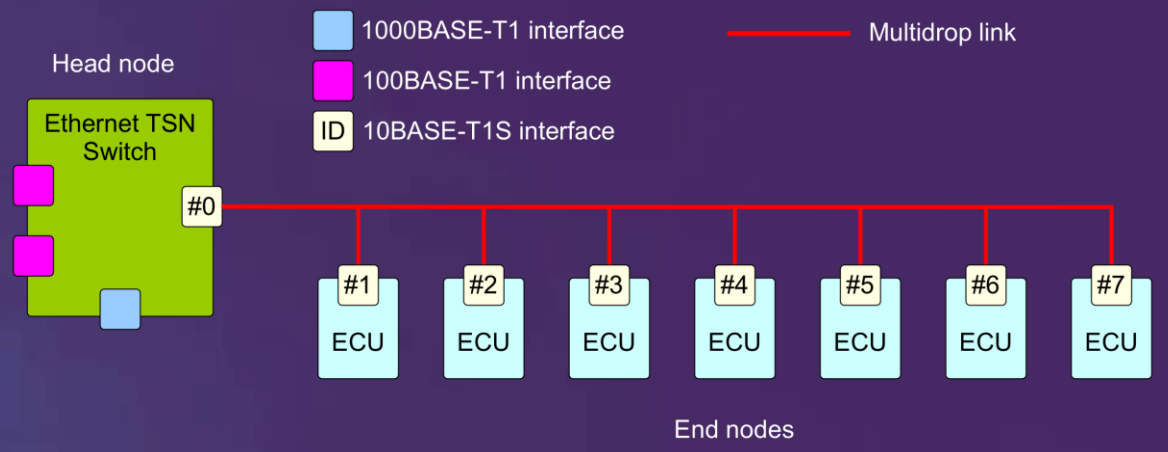
- Guaranteed window
  - Within an open window
  - No overlappings among distinct priority queues from a single interface
  - In the worst-case, a frame transmission can start anytime within a guaranteed window
  - Max length: window length – guard band length
  - Min length: zero



[2] L. Zhao and P. Pop and S. S. Craciunas, “Worst-Case Latency Analysis for IEEE 802.1Qbv Time Sensitive Networks Using Network Calculus,” IEEE Access, vol. 6, pp. 41 803–41 815, 2018.

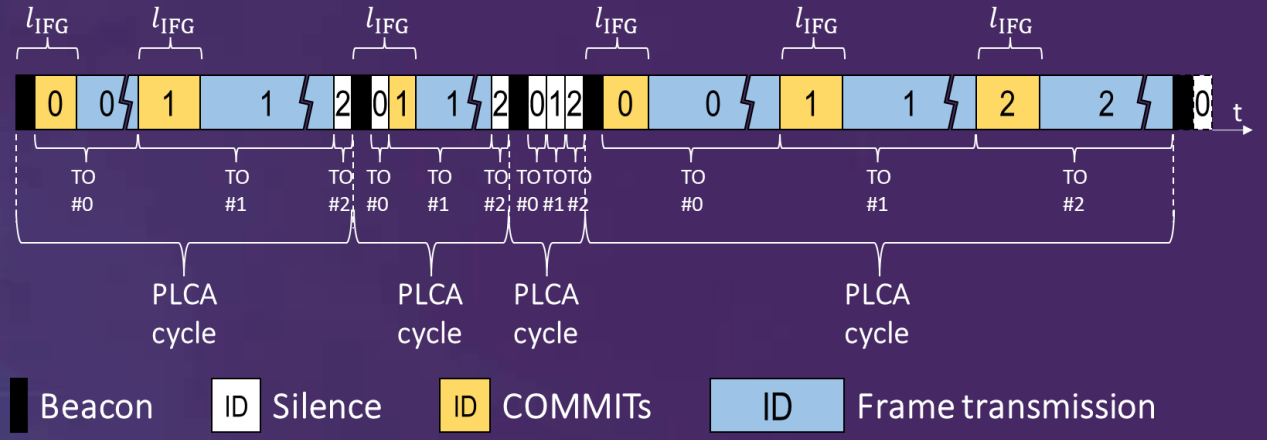
10BASE-T1S

- Single Pair Ethernet
- Half-duplex Multidrop
- Up to 8 nodes
- Physical Layer Collision Avoidance (PLCA)
  - Avoids frame collisions
  - Provides bounded latency
    - No more exponential random wait time from CSMA/CD due to collisions
      - CSMA/CD is a MAC feature
      - Collisions are avoided in the PHY
  - Optimal bandwidth utilization
    - No waste in transmission time
  - Guaranteeing fairness among nodes

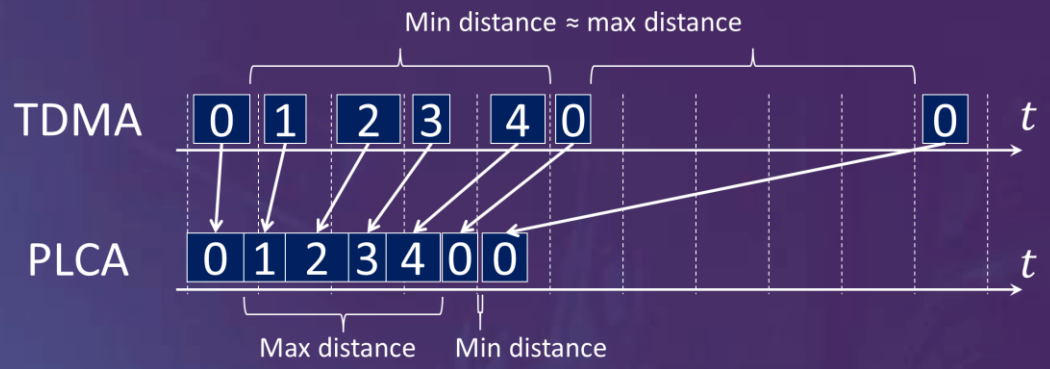


Physical Layer Collision Avoidance (PLCA)

- Frame transmissions within a Transmit Opportunity (TO)
  - Each node has a single TO per PLCA cycle
- Two modes for transmission
  - Normal mode
  - Burst mode
- Silence when there is no frame to transmit
- Commit symbols are transmitted just before frame transmission when beacon and silence is shorter than an IFG



Min distance ≈ max distance ≈ (nodes – 1) * max packet/slot length



Min distance ≈ 0, max distance ≈ (nodes – 1) * max packet length

Shortest PLCA cycle

- Silence from all nodes

Longest PLCA cycle

- Transmissions of max frame size from all nodes

Figures adapted from Figures 5.39 and 5.40 from [1] K. Matheus and T. Königseder, Automotive Ethernet, 3rd ed. Cambridge University Press, 2021.

TAS + PLCA

Best of the two worlds?!

- Time-Aware Shaper
- 10BASE-T1S PLCA

Ultra-low latency, jitter, and loss on half-duplex multidrop links?!

They are cyclical but not synchronized

- TAS is TDMA-like
- PLCA is Weighted Round-Robin (WRR)-based
- Both can work together
  - Mistakes in the planning of TAS or PLCA parameters may cause packet loss or even starvation

TAS + PLCA

The choice of a TAS scheduling is not an easy task

- TAS on 10BASE-T1S PLCA is harder

Deterministic systems require certification

- Performance guarantees
- Worst-case analysis
  - Deterministic Network Calculus

Providing optimal TAS scheduling is hard

- PLCA is not aware of frame priority
- All scheduled traffic flows must be compliant
- A tool is required for calculating worst-case bounds

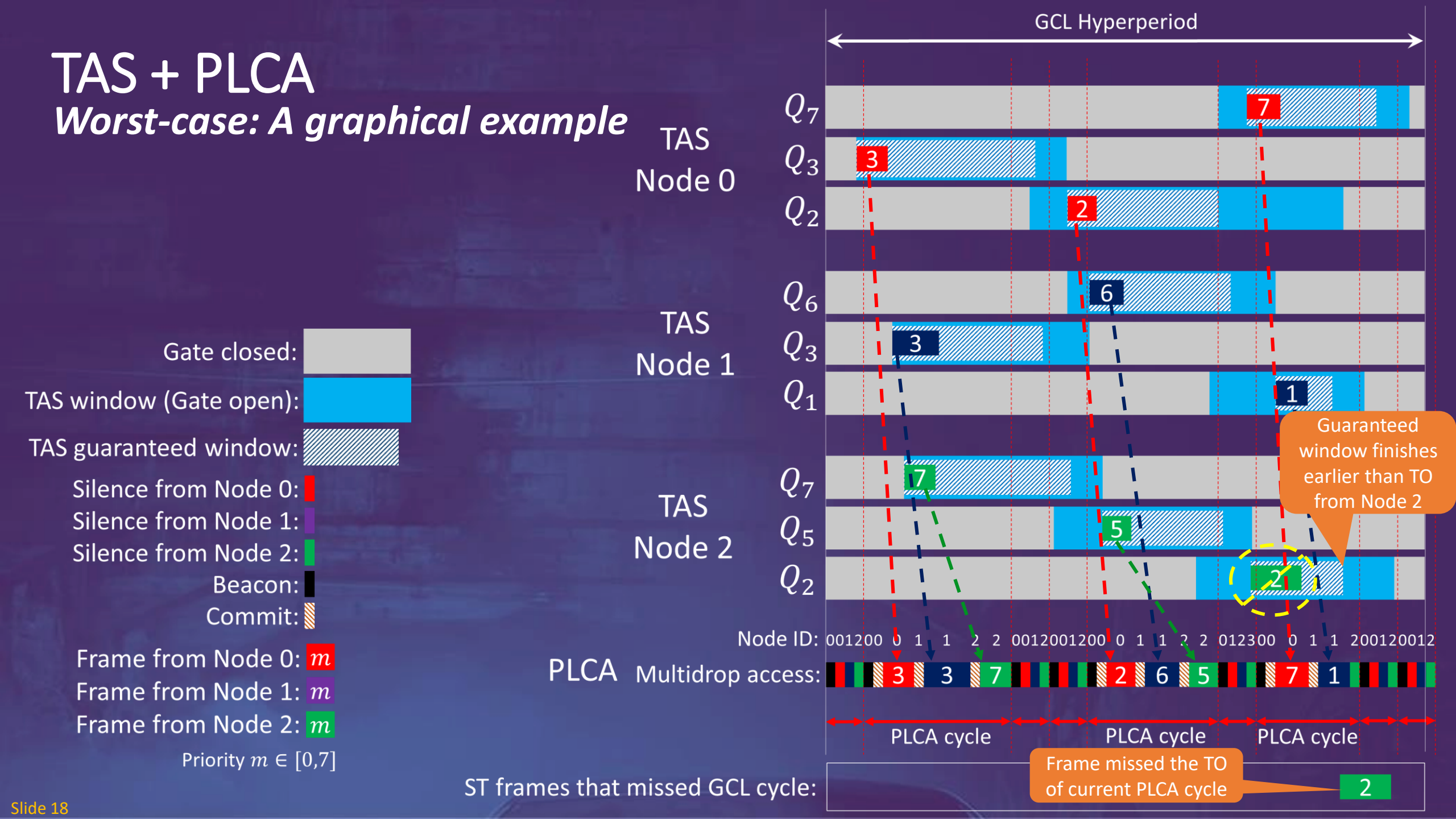
There was neither an analytical solution nor an open-source tool for calculating the worst-case bounds of systems with TAS and PLCA

- We provide both[3]

[3] David A. Nascimento and Steffen Bondorf and Divanilson R. Campelo, “Modeling and Analysis of Time-Aware Shaper on Half-Duplex Ethernet PLCA Multidrop”. *IEEE Transactions on Communications*, 71(4):2216–2229, 2023.

TAS + PLCA

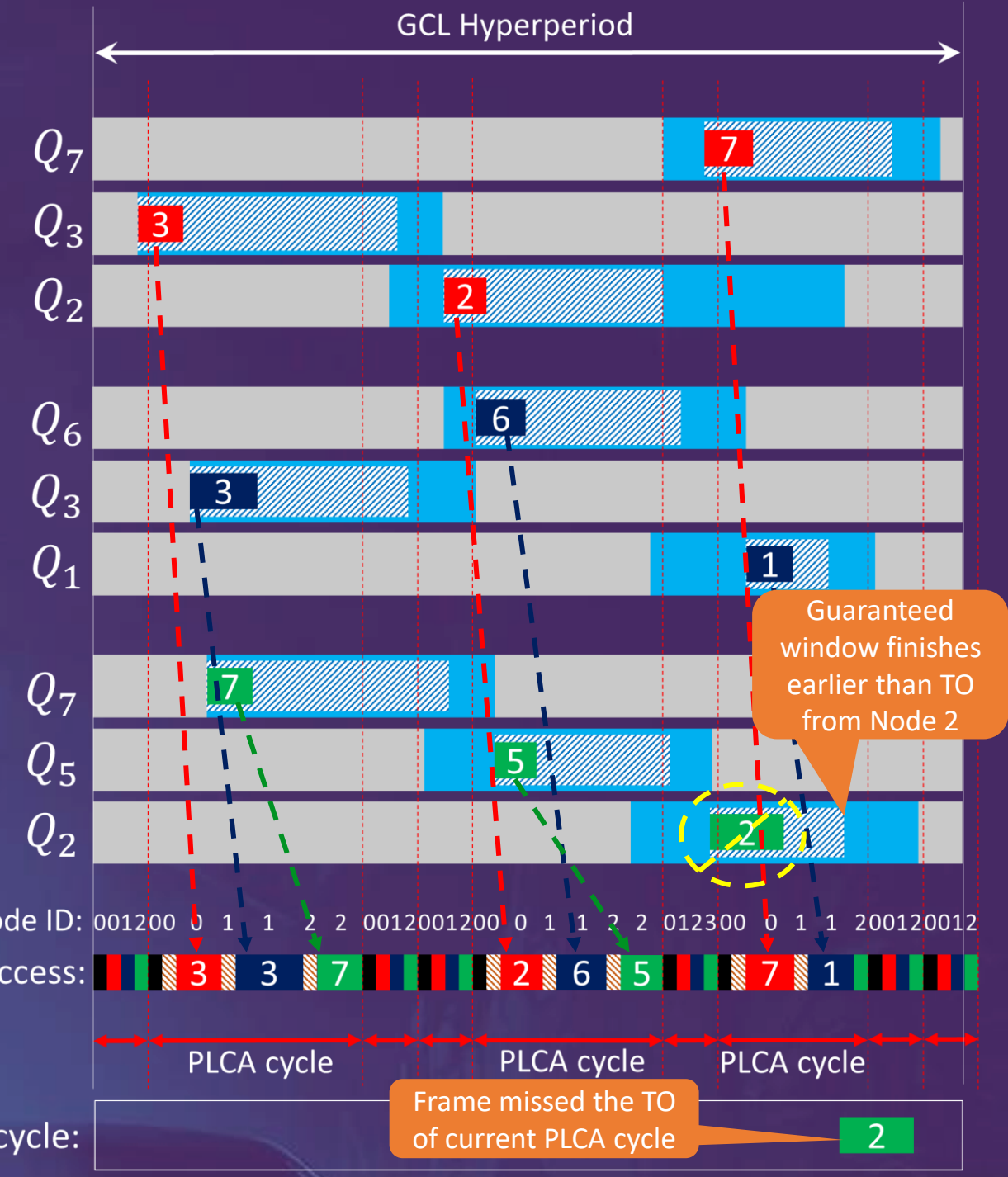
Worst-case: A graphical example



TAS + PLCA

In a worst-case situation

- A frame is transmitted last within a PLCA cycle composed of frames from overlapping guaranteed windows among distinct nodes
  - Worst-case WRR behavior
- **A PLCA cycle must fit within a guaranteed window**
  - Otherwise a frame can miss its open window
    - Deadline is not met



TAS + PLCA

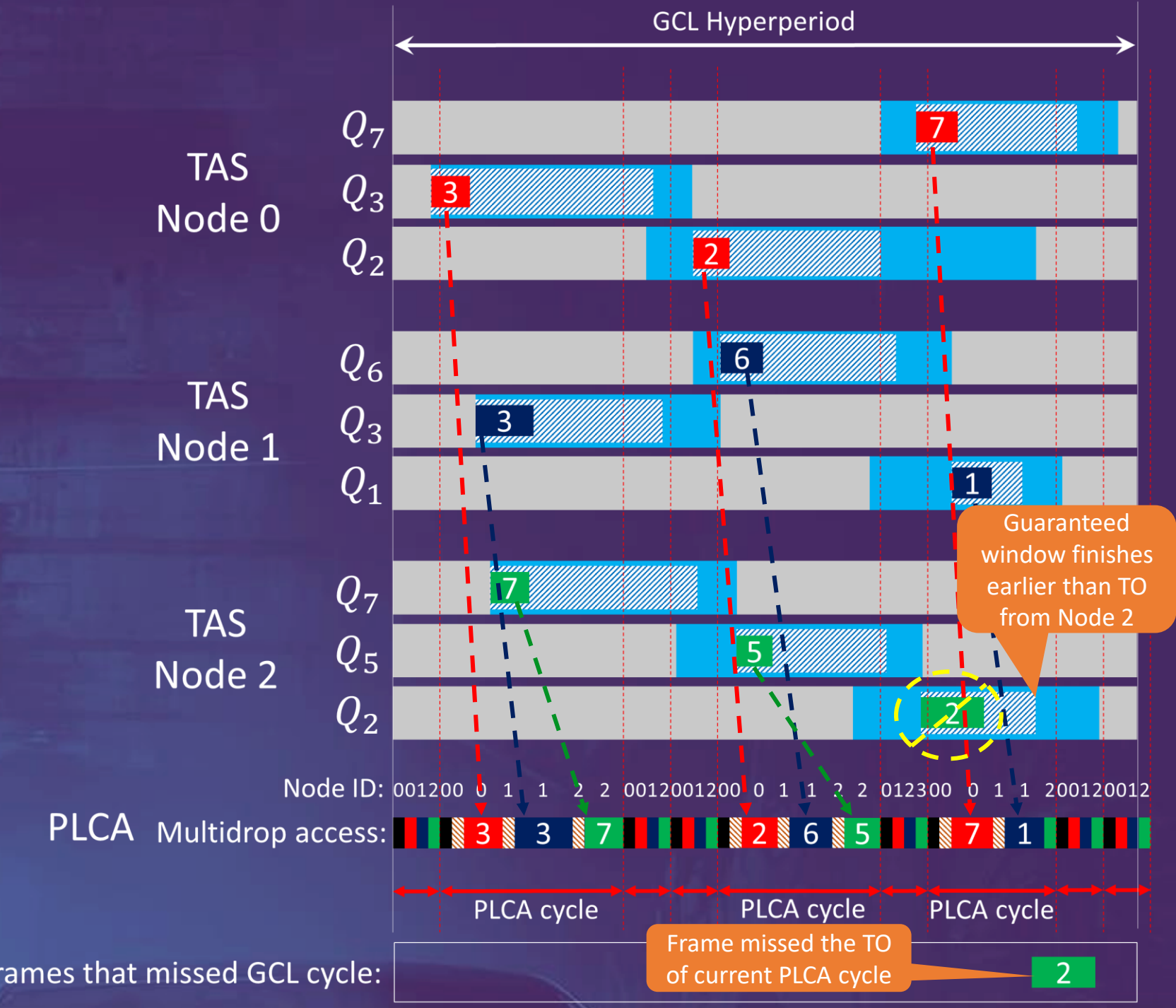
TAS scheduling shall have few overlapping guaranteed windows among distinct nodes

Fewer overlappings

- Shorter PLCA cycles
- Lower bounds

No overlappings

- The best situation
- Lowest wait time for transmission
- PLCA cycle is composed of a frame from the current node and silence from the other nodes



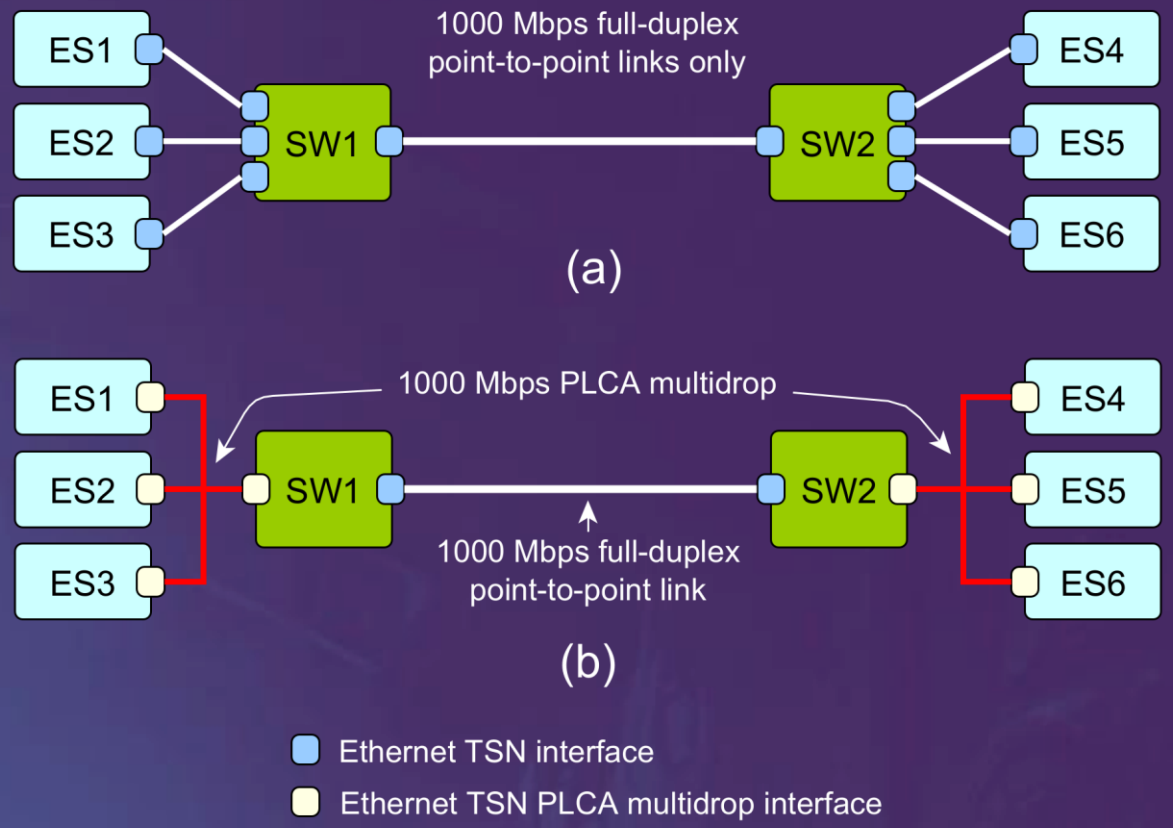
Full-duplex switched Ethernet *vs* Half-duplex PLCA Multidrop Ethernet

- 13 distinct TAS scheduling cases[2]
  - Different overlapping scenarios, lengths of open window, open-close cycles, and priority assign
- 13 scheduled traffic flows[2]
- e.g.:

Frame size (bytes)	Period (μs)	Deadline (μs)
400	250	8908.0
400	250	56935.0
400	250	35879.0
400	250	170198.0

foi

- Hypothetical "1000BASE-T1S"[3]
  - Sum of flows bandwidth exceeds 100 Mbps
- Worst-case delay analysis
  - Network Calculus



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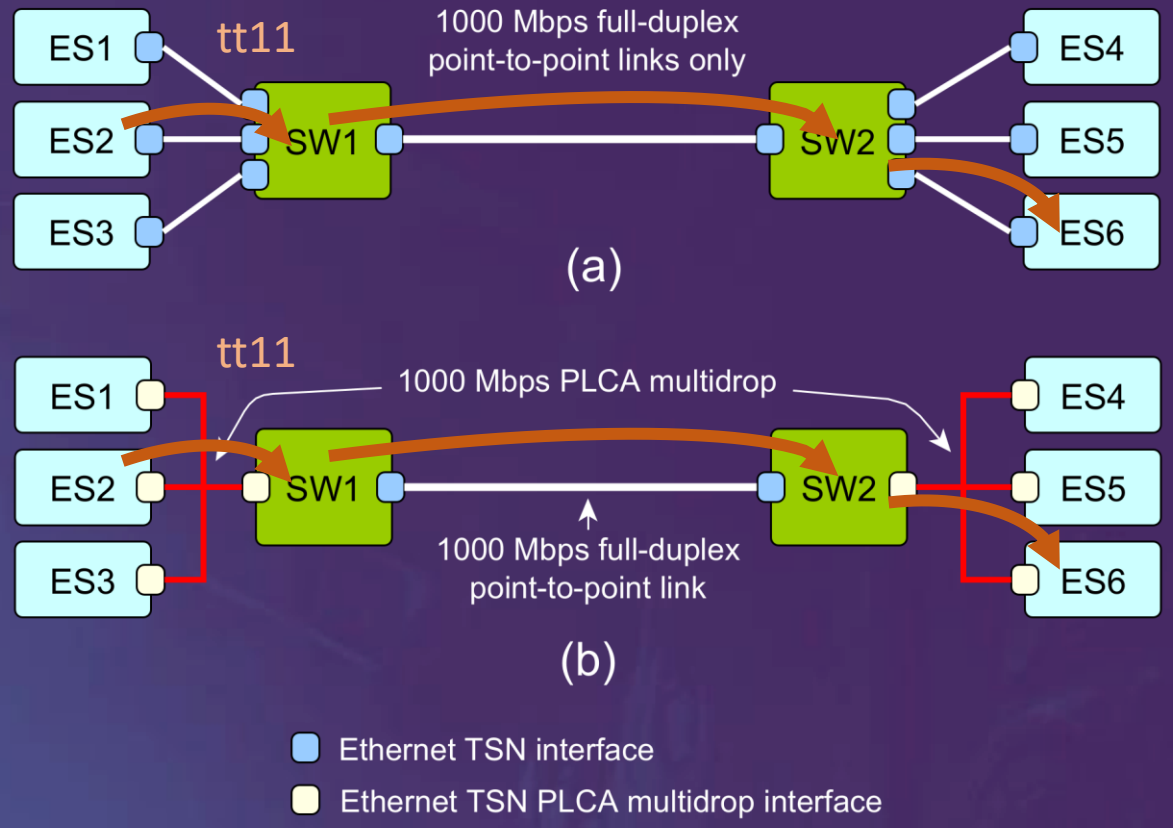
Full-duplex switched Ethernet *vs* Half-duplex PLCA Multidrop Ethernet

Results

- Flow of interest (foi)
  - As expected, there was an increase on delay bounds
  - Increase ranges from 10.7% to 27.6%[3]
  - Below the deadline



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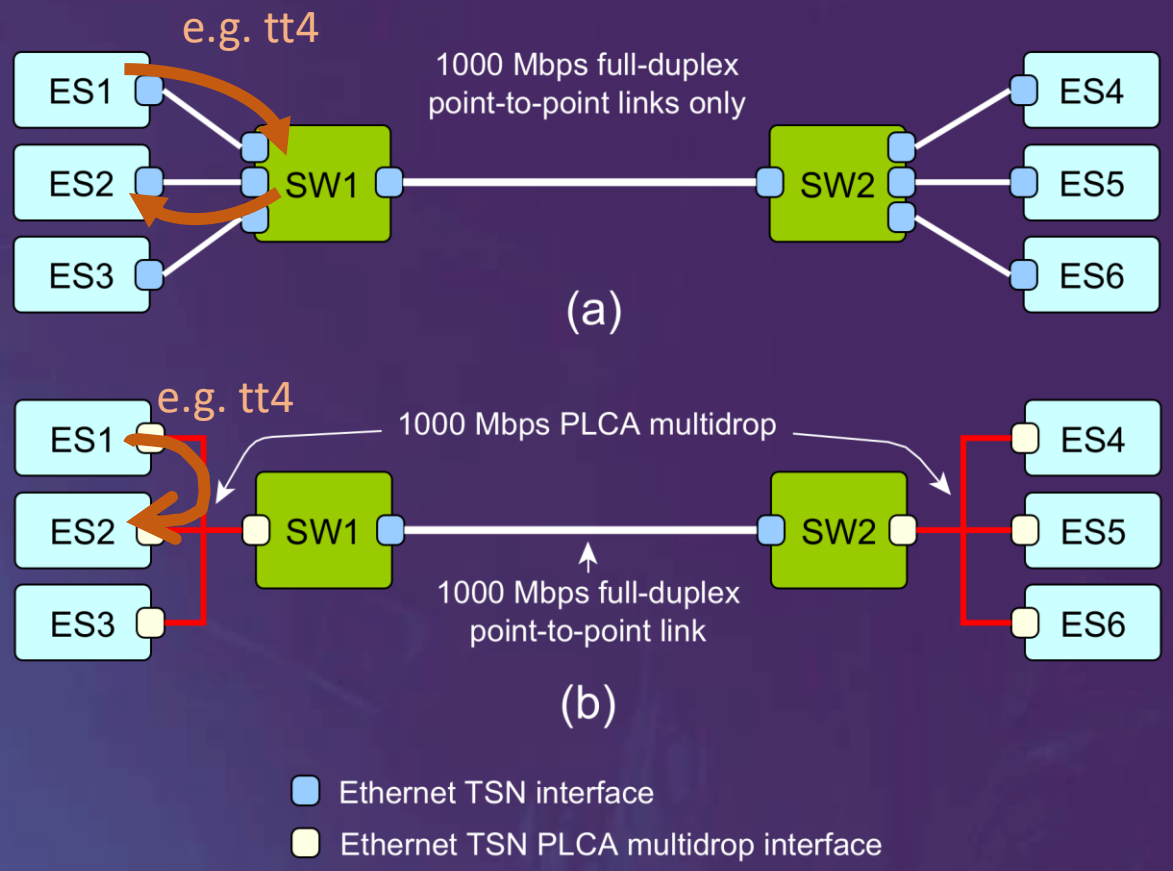
Full-duplex switched Ethernet *vs* Half-duplex PLCA Multidrop Ethernet

Results

- 5 of 13 scheduled traffic flows with source and destination ES in the same multidrop
  - All 5 flows have a reduction in delay bounds when using a single-hop PLCA multidrop instead of two hops of full-duplex links[3]
  - Decrease ranges from 16.7% to 33.2%[3]



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Conclusion

TAS and 10BASE-T1S PLCA

- Ultra-low latency on half-duplex multidrop links
- Reliable and cheaper solution
  - Less PHYs than full-duplex switched
- End-to-end transmissions of scheduled traffic Ethernet flows
- Available models and tools for analyzing TAS scheduling over 10BASE-T1S PLCA multidrop
- “Ubiquitous Ethernet In-Vehicle Networks”

Future works

- Worst-case jitter analysis
- Analysis of more use cases:
  - Automotive networks with 10BASE-T1S
  - 10BASE-T1S PLCA without TAS
- Integration of 10BASE-T1S PLCA with other TSN protocols
  - E.g., Asynchronous Traffic Shaping (ATS) – IEEE 802.1Qcr

Thank you