Inter-processor Connectivity for Future Centralized Compute Platforms

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Agenda

• In-vehicle networking trends
• The ‘All Ethernet’ network
• Ethernet challenges
• Introduction to PCIe
• Key PCIe switch features
• Inter-Processor connectivity use case
• Conclusion
In-vehicle networking trends

Decentralized, hardware defined

- Multiple application-specific buses
- Distributed gateways
- Domain-specific ECUs
- Ineffective security
- Complex wiring harness up to 5km

Homogeneous, software defined

- Zonal ECUs with centralized compute platform
- IP-based, Ethernet IVN
- Software-oriented architecture

Powerful, flexible in-vehicle network is required to meet autonomous challenges

Image source: Audi, Automobil-Elektronik Kongress, Ludwigsburg 2018
Vision - ‘All Ethernet’ network
Zonal ECU with centralized compute platform

- Standards based, homogeneous network from Mbps to multi-Gbps
- Proven, secure IP communication protocols from cloud to device
- Removes need for complex gateways – seamless communication
- Reduces verification and validation efforts, wiring cost, weight and installation complexity

Ethernet is the enabler for connected and autonomous vehicles
Ethernet challenges

Zonal ECU accumulated bandwidth

- HD Camera (>10Gbps)
- Radar/Lidar (1Gbps)

Managing vast network data bandwidth across central compute SoC(s)

• IEEE 802.3cy required
Ethernet challenges
Centralized compute interconnect

- PCIe is the interface of choice for High-performance compute SoC
- Ethernet vehicle network and timing

PCle switch required for inter-processor connectivity

\(<\text{PCIeGen}> \times <\#Lanes> \text{ eg. } 5x2 = \text{PCIe Gen}5 \times 2 \text{ Lanes}\)
Introduction to PCIe

- PCIe is a point-point high-speed component interconnect specified by PCI-SIG group
  - Bandwidth of a PCIe port can scale by increasing bit rate per lane (PCIe Gen), or increasing number of lanes in a port

- Uses address based routing for I/O
  - Memory semantics used by host and end points, no complex I/O driver stack overhead gives minimal latency

- PCIe domains are closed topologies
  - Only known, enumerated devices can communicate within a system

- Peer-peer I/O between end point devices connected to a PCIe switch is supported
  - Access Control Services (ACS) optional feature to limit peer-peer I/O for added security

PCIe is a secure, low latency, scalable high-bandwidth interconnect
Introduction to PCIe

• Packets are ACK or NAK to confirm good reception
  • NAK or ACK_timeout forces transmitter replay of packet

• Credit based flow control mechanism
  • TX knows if RX buffer has space to receive a packet

• Advanced port status and error checking
  • Link and end-end CRC checksum
  • Error correction
  • Link and Port status change interrupts and Advanced Error Reporting (AER) supported

PCIe guarantees error-free packet transmission
Key PCIe switch features

**PCIe Virtual Switch Partitions (VSP)**

- Divide PCIe switch into Virtual Switch Partitions (VLAN Analogy)

- Each partition:
  - Has its own root complex
  - Is a closed system with individual Enumeration and partition reset schemes

- Provides isolated memory address islands

- Dual port storage devices give transparent access to two hosts
Key PCIe switch features

PCIe Non-Transparent Bridging (NTB)

- NTB provides limited memory windows between partitions.
- NT End Point (NT EP) function is enumerated in each NT enabled partition.
- R/W’s towards an NT EP memory window are translated to alternate host memory region.
- Only provisioned devices can access the NT EP.
- NTB driver protects a host by completely controlling all EP device access, irrespective of the EP device native HW capabilities.
Key PCIe switch features

PCle Multicast (MC)

- PCIe multicast can send posted information from any source port to a group of destination ports
- Multicast is supported with NTB
- Multicast address regions can be statically defined
Inter-Processor connectivity use case

- PCIe features of VSP, NTB, MC enable a flexible, modular, secure communication interconnect within a centralized compute platform.
- PCIe switches provide chip interconnect with the scalable necessary bandwidth, lowest latency (100ns) and a strong committed ecosystem and roadmap.
- Multiple processors can access the same endpoint concurrently (e.g., SSD, Ethernet bridge).

Modern PCIe switches enable complex data path routing configurations.
Conclusion

- The next-generation vehicle is a data center on wheels. CPU, MPU, GPU, NAD, SoC, accelerators, storage ... all natively wanting to communicate PCIe!
- PCIe switches connect all processors within the central computer, meeting the connectivity bandwidth demands whilst enabling platform modularity, scalability, secure design partitioning and bridging to the Ethernet domain
- Ethernet provides the vehicle network, including transport of sensor data and timing to all devices in the central computer

**PCIe switching and Ethernet – the winning combination**