Automotive Physical Layer System Design for High Bandwidth Protocol

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Background

- High speed data links are not new concepts to automotive. However, they were contained and implemented on a few unique systems (e.g. High resolution display and surround view camera, Radar etc.)

- New vehicle features like Driver Assist, Cloud Connectivity, Autonomous Vehicles, etc. now require high speed links between modules. Implementing such features with unique dedicated links is not a feasible solution and they can't be supported using current traditional networks (e.g. CAN/CANFD, LIN, FlexRay, etc.).

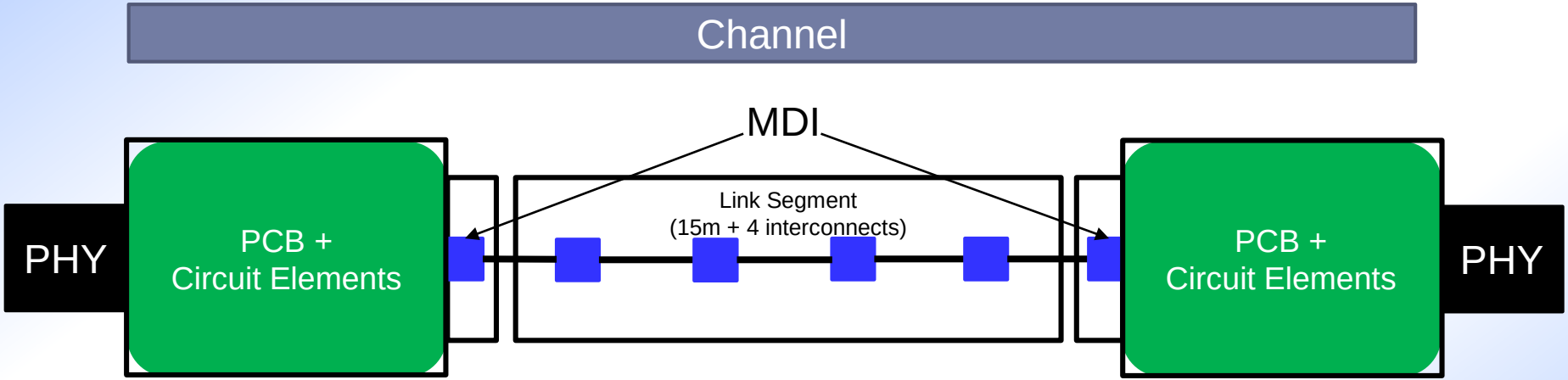
- Due to these demands, faster network communication protocols with higher bandwidth are being adopted/integrated into vehicles architecture.

High Bandwidth Network Design

- Integrating high bandwidth protocols in a distributed network entails that every network node must now be designed with high frequency and RF performance in mind.
- These modules must consider:
  - Signal Integrity (SI) Channel Requirements
    - Controlled PCB Design
    - Controlled Link Segment (Cable/Connector Assembly) Design
    - Signal Integrity Budget Allocation
  - Automotive EMC Requirements

Automotive companies face new challenges in physical layer design by adopting high bandwidth network protocols.

Physical Layer Overview



- PCB: Printed Circuit Board
- MDI: Media Dependent Interface (PCB Connector)
- Link Segment 15m + 4 inlines is longest desired length (Not necessarily the most feasible length)

Scattering Parameters (S-Parameters) Definitions

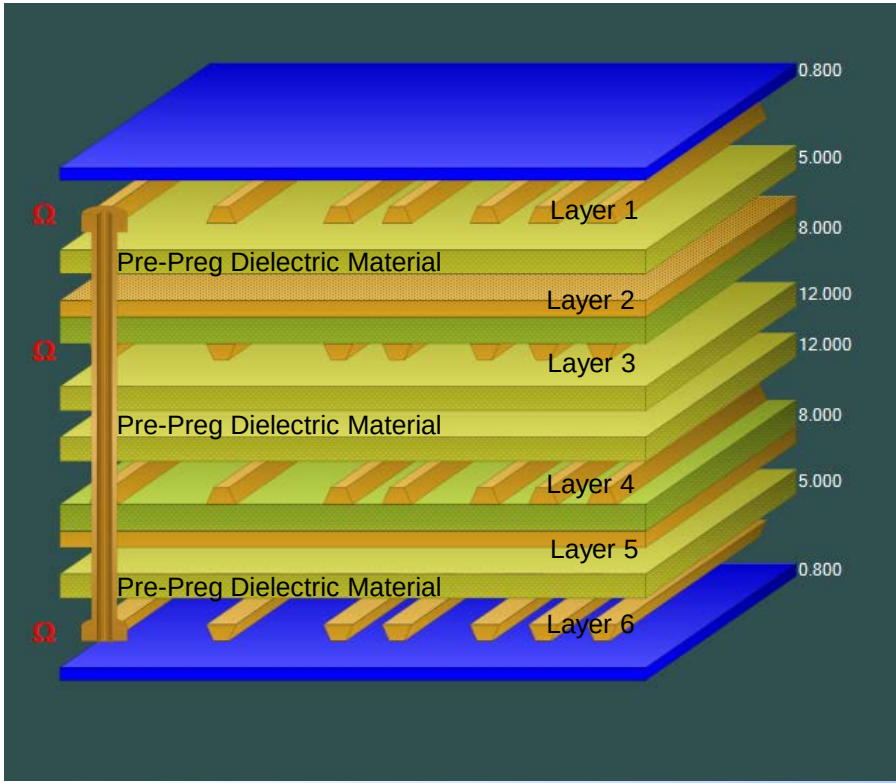
- Return Loss: Signal loss due to a discontinuity in the transmission line (e.g. Impedance mismatch)
- Insertion Loss: Signal loss due to the insertion of a transmission line (e.g.: PCB trace, cable, connector, etc.) and circuit components.
- Mode Conversion: Signal Loss due to imbalance in the transmission line
- Coupling/Crosstalk Loss: Signal loss due to noise coupling (near/far end)

PCB Design Requirements

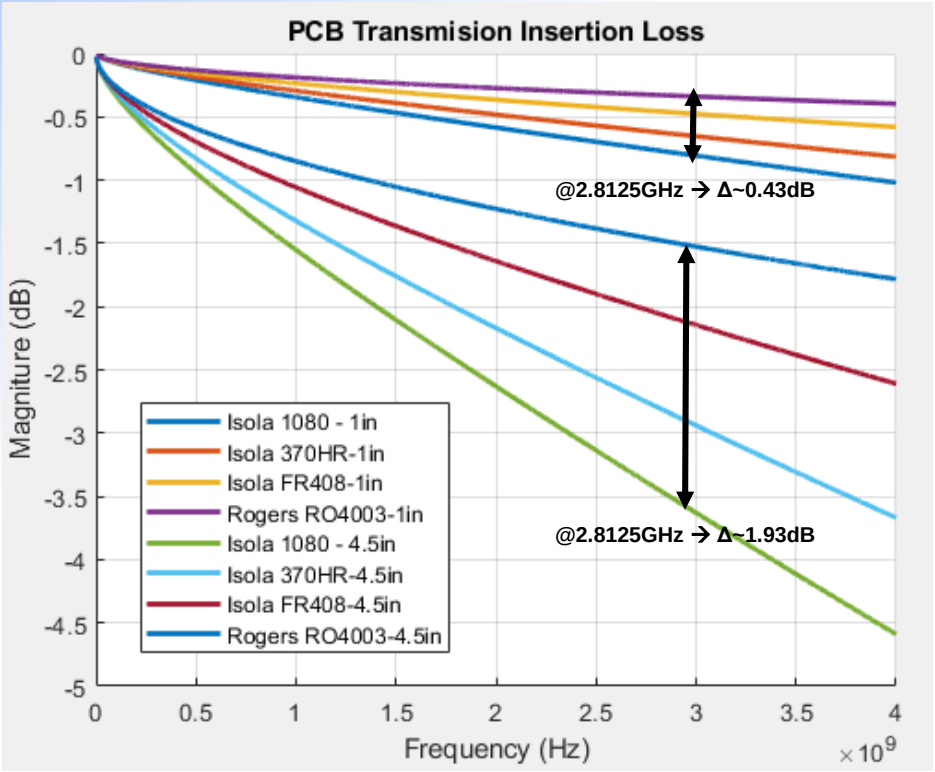
- PCB Stackup
  - Minimum Layer Count, 4-layer stack-ups might be a thing of the past
- Use of Low loss FR4 Material
- High Frequency PCB Layout Practices
  - Choosing an Optimum Waveguide Structure
  - Signal Integrity Requirements
  - EMC Mitigation

6-Layer PCB Stack up Overview

- Use symmetry in the stack up (e.g. if layer 2 is ground then layer 5 should be ground)
- Use of Mixed layers (e.g. Power Islands and signals)
- Define high speed routing Layers/controlled impedance layers. This will help with tuning the height of dielectric to the corresponding reference planes
- Define via types (e.g. through hole, back drilled, blind, micro, etc.)
- Define material type for dielectric coefficient and dissipation factor



PCB Material Loss Comparison



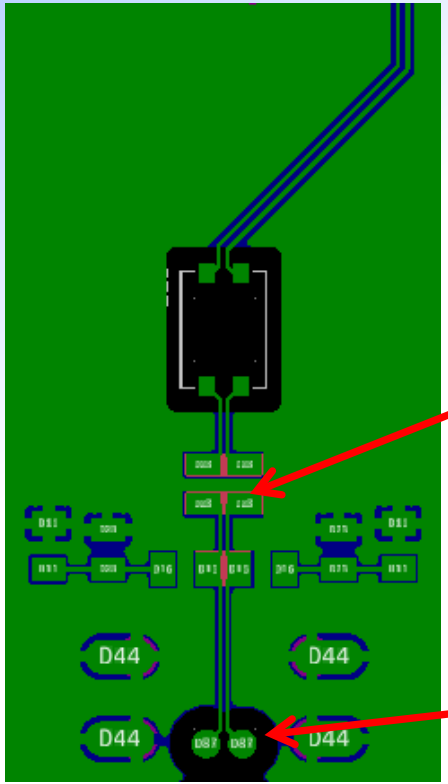
Better

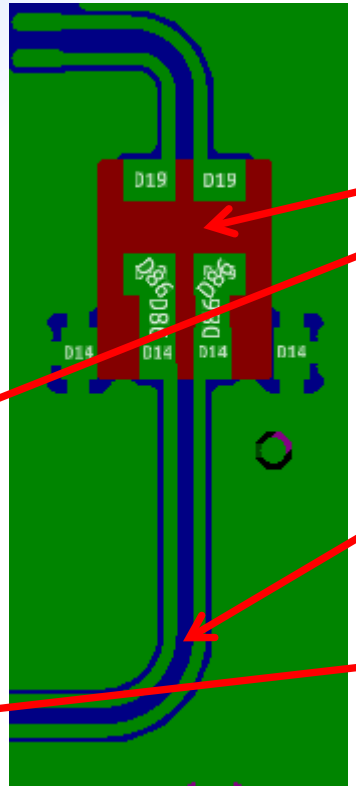
Worse

- For 100BASE-T1/1000BASE-T1, PCB losses are not as significant due to the lower frequencies; however additional losses are added from the circuit components (e.g. CMC)
- For MultiGBASE-T1 and Beyond 10G, PCB losses become more significant due to the higher frequencies. Now losses shall be considered for both PCB traces and possible circuit components (e.g. CMC)

$$IL_{1080} = 0.18\sqrt{f(GHz)} + 0.1650f(GHz) \text{ dB/in}$$
$$IL_{370HR} = 0.18\sqrt{f(GHz)} + 0.1138f(GHz) \text{ dB/in}$$
$$IL_{FR408} = 0.18\sqrt{f(GHz)} + 0.0559f(GHz) \text{ dB/in}$$
$$IL_{RO4003} = 0.18\sqrt{f(GHz)} + 0.0091f(GHz) \text{ dB/in}$$

PCB Layout Practices – High Frequency



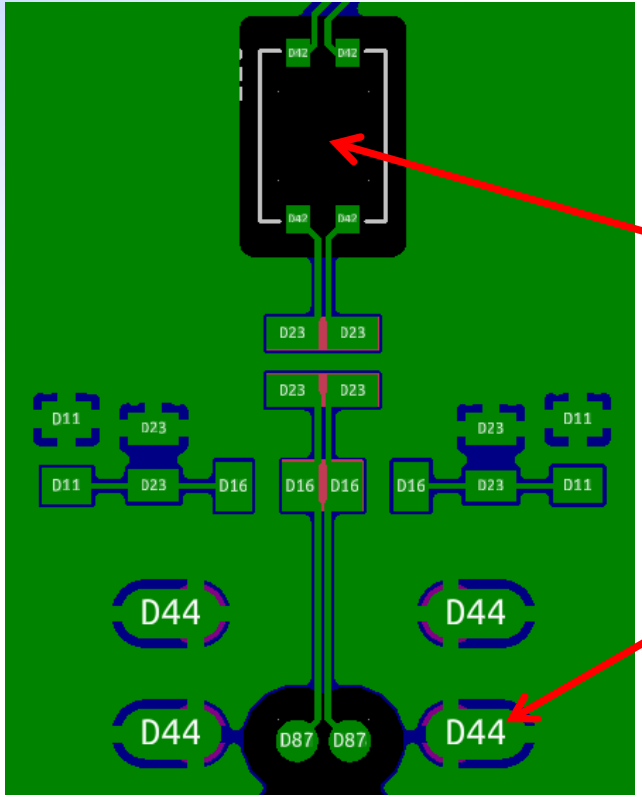


- ❖ No ‘T’ stub connections
- ❖ Remove copper underneath component pads

- ❖ Use of Symmetry in board traces
- ❖ Avoid use of 90° sharp corners

- ❖ Connector signal integrity analysis with selected Stackup for optimum footprint.
- ❖ Connector manufacturing requirement analysis

PCB Layout Practices – EMC Mitigation



- ❖ Remove Copper from underneath CMC
- ❖ Shield termination strategy for optimum electrical performance.

Link Segment Requirements

- IEEE specification defines link segment requirements
  - Signal Integrity
    - Return and Insertion Loss
    - Mode Conversion
    - Near and Far End Crosstalk
    - Shield Effectiveness
  - Environmental

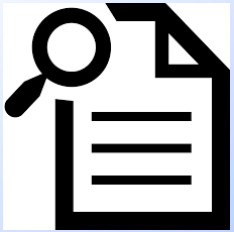
Before an assembly is evaluated for SI performance;
Ford requires these components to meet environmental requirements.

Signal Integrity Evaluation Process

Connector suppliers must pair their connector with a cable for optimum impedance control

Validate Link Segment Signal Integrity

Characterize the cable-connector assembly against the protocol budget

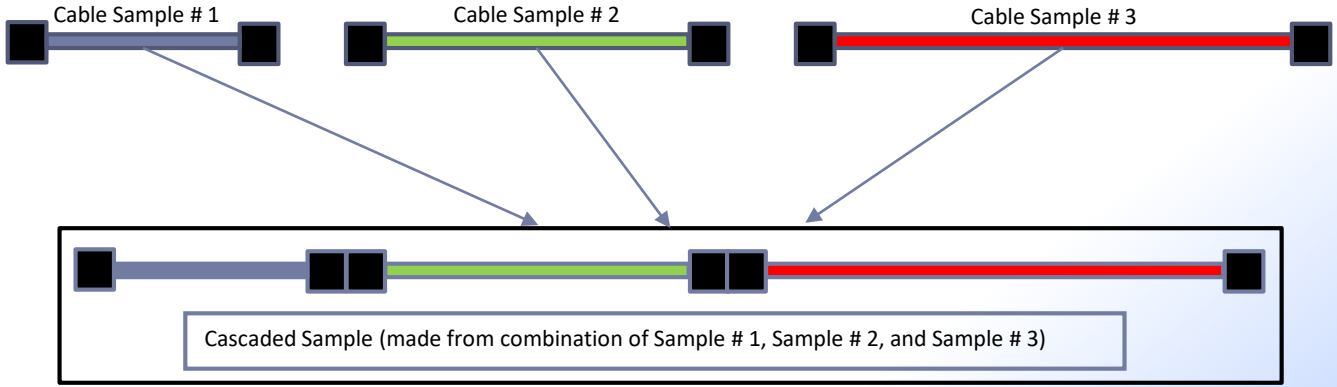


Ford Analysis Sample List

- 0.2, 0.5, 1-10 meter cable with no interconnects
- 1 meter cable with 4 equally spaced interconnects
- 1.7 meters cable with no interconnects
- 15 meters cable with 4 equally spaced interconnects

Link Segment Evaluation

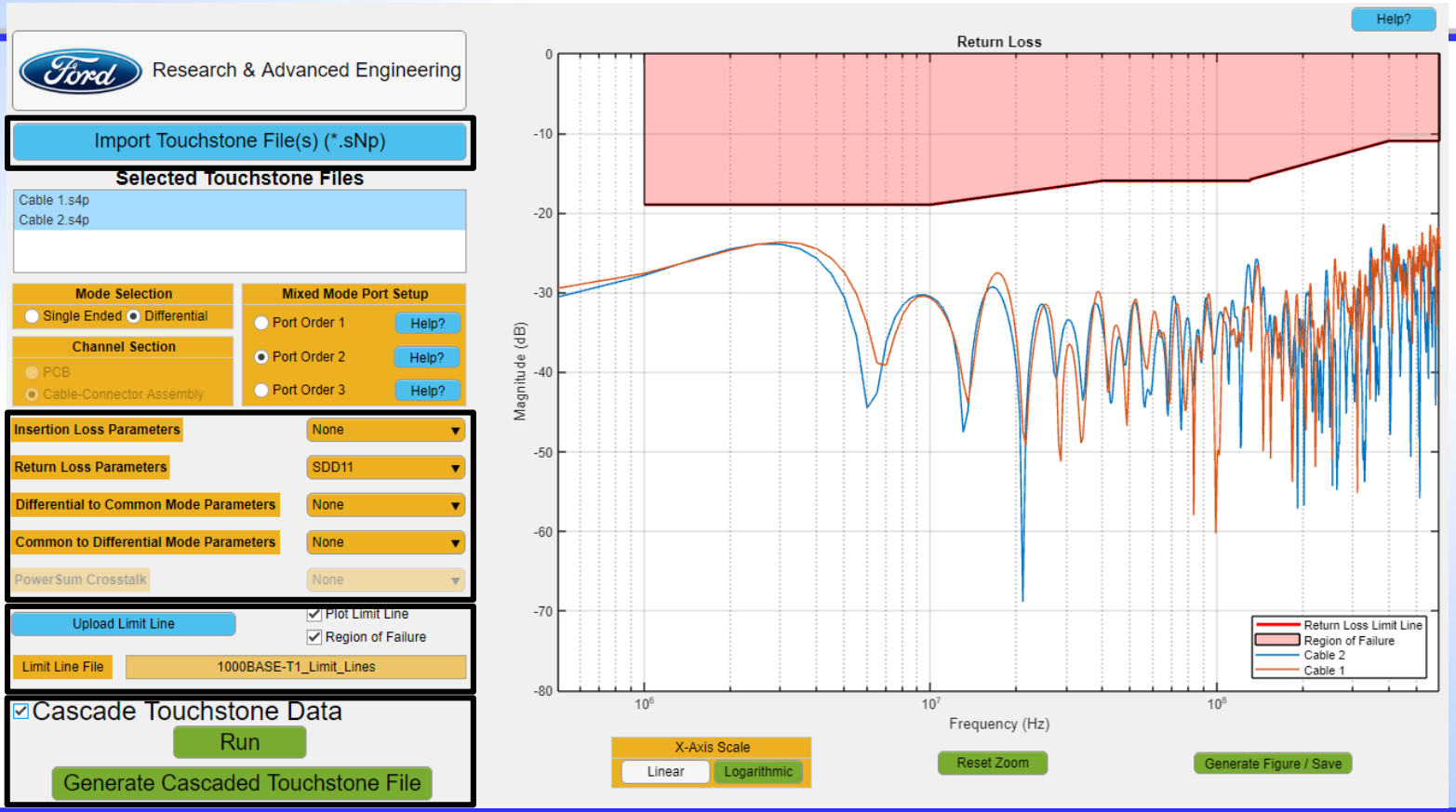
- Ford is building a library of captured S-Parameter data of multiple segment lengths (0.2m, 0.5m, 1-10m). The captured data is utilized to simulate cable assemblies of different configurations and determine signal integrity performance.



Link Segment Evaluation

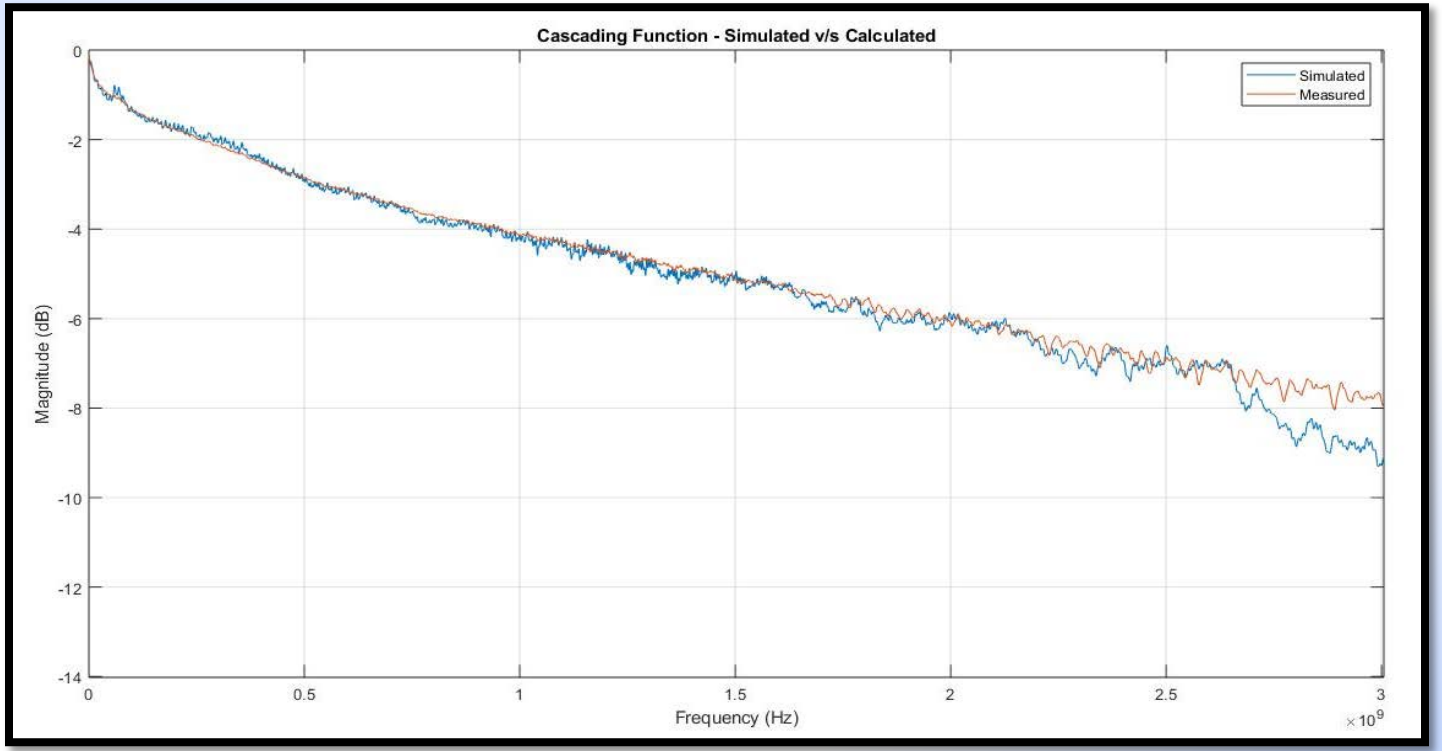
- 1 meter cable with 4 equally spaced interconnects
  - This link will assess the worst case **return loss** and determine the shortest segment between two interconnects in a link segment assembly
- 1.7 meters cable with and without an inline
  - For **EMC testing** only
- 15 meters cable with 4 equally spaced interconnects
  - This assembly will assess the worst case **insertion loss** of a link segment. This will determine whether 15m and 4 inner connects with a low loss cable can meet the allocated loss budget.

Signal Integrity Analysis Tool



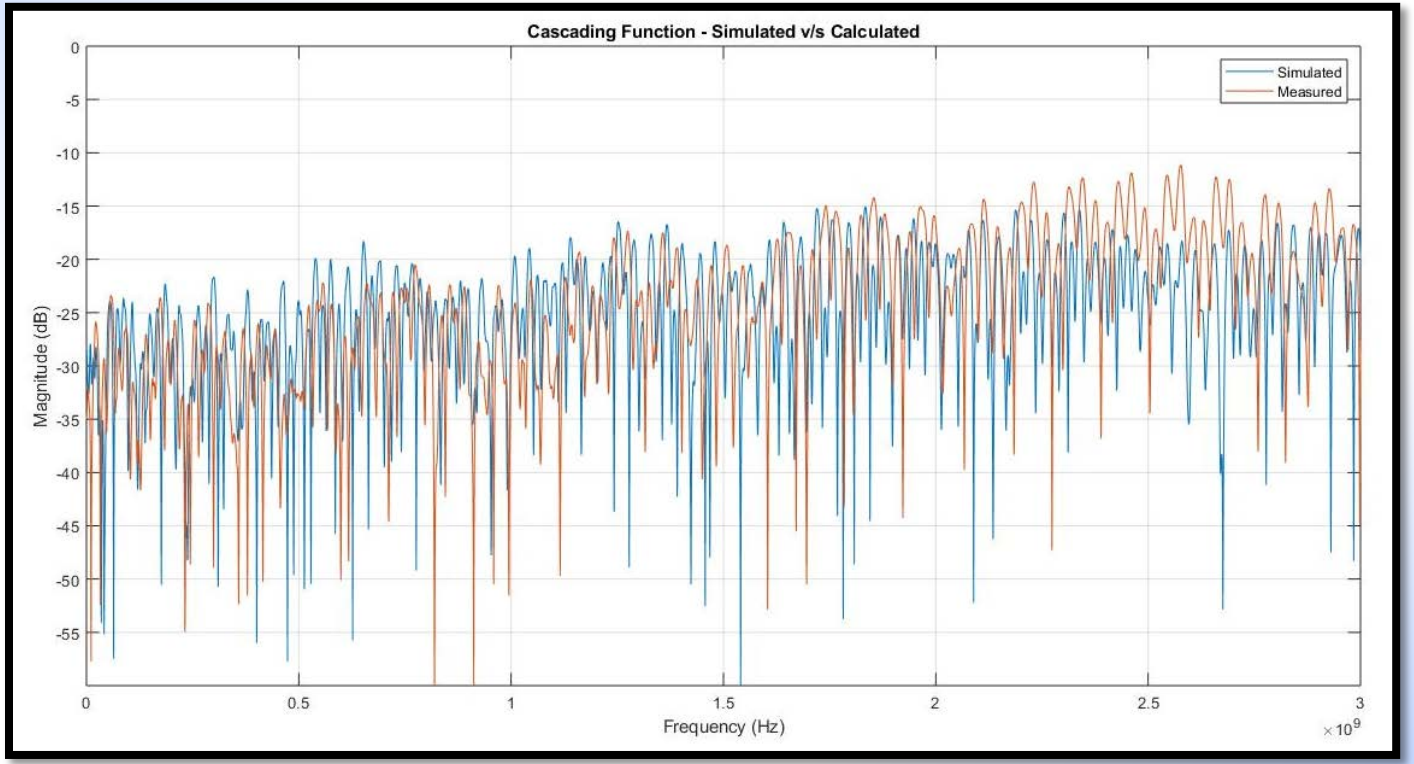
Cascade Analysis Capability

Cascaded Insertion Loss – Simulated v/s Measured



Cascade Analysis Capability

Cascaded Return Loss – Simulated v/s Measured



Conclusion

- From analysis, it is prudent that we consider allocating budgets for different segments of the link (i.e. separate budget for PCB and Cable-Connector assembly)

- Currently there is an Ad-Hoc for IEEE802.3ch to incorporate an informative annex detailing PCB losses. This is a step in the right direction to ensure that we account for the entire link.

Questions / Discussion