

IEEE Std 1800™-2017
(Revision of
IEEE Std 1800-2012)

Errata to IEEE Standard for SystemVerilog— Unified Hardware Design, Specification, and Verification Language

Sponsor
Design Automation Standards Committee
of the
IEEE Computer Society
and the
IEEE Standards Association Corporate Advisory Group

Correction Sheet
Issued 15 April 2019

Copyright 2019 by the Institute of Electrical and Electronics Engineers, Inc. All rights reserved. Published 2019.
Printed in the United States of America.

This correction sheet may be freely reproduced and distributed in order to maintain the utility and currency of the underlying Standard. This correction sheet may not be sold, licensed or otherwise distributed for any commercial purposes whatsoever. The content of this correction sheet may not be modified.

In Clause 4, page 61, change numbering of subclause 3.4.1 as follows:

4.4.1 Active region sets and reactive region sets

In Clause 4, page 61, change the references of 3.4.2 and 3.4.3 to 4.4.2 and 4.4.3, respectively, as follows:

In addition to the active region set and reactive region set, all of the event regions of each time slot can be categorized as *simulation regions* (see 4.4.2) or *PLI regions* (see 4.4.3).

In Clause 4, page 61, change numbering of subclause 3.4.2 as follows:

4.4.2 Simulation regions

In Clause 4, page 62, change numbering of subclause 3.4.3 as follows:

4.4.3 PLI regions

In Clause 4, page 67, change the final reference in subclause 4.9.1 as follows:

This includes implicit continuous assignments inferred from port connections (see 4.9.6).

In Clause 4, page 68, change numbering of subclause 3.9.6 as follows:

4.9.6 Port connections

In 12.4.2.1, page 302, change reference of 3.4.1 to 4.4.1 as follows:

The descriptions in 12.4.2 mention several cases in which a violation report shall be generated by unique-if, unique0-if, or priority-if statements. These violation checks shall be immune to false violation reports due to zero-delay glitches in the active region set (see 4.4.1).

In 12.5.3.1, page 308, change reference of 3.4.1 to 4.4.1 as follows:

The descriptions in 12.5.3 mention several cases in which a violation report shall be generated by uniquecase, unique0-case, or priority-case statements. These violation checks shall be immune to false violation reports due to zero-delay glitches in the active region set (see 4.4.1). The violation reporting can be controlled by using assertion control system tasks (see 20.12).

In 14.14, page 346, change the third paragraph as follows:

The following is an example of a `global clocking` declaration:

```
module top;
  logic clk1, clk2;
  global clocking sys @(clk1 or clk2); endclocking
  //...
endmodule
```

In A.10, change footnote 7 as follows:

In a `parameter_declaration` that is a `class_item`, the `parameter` keyword shall be a synonym for the `localparam` keyword.