

IEEE Electronic Design Automation Standards Collection: VuSpec™

The 2007 IEEE Design Automation VuSpec is a must have item for embedded software developers, analysts, marketing & sales professionals, and students who want to get up to speed on the full library of international EDA Standards.

Semiconductors, wired or wireless communication systems, electronics, medical test equipment, and the entire EDA software industry itself rely on these recognized standards covering Logic, Design, Simulation, RTL & Formal Verification, IP/Cores, ALF, ASIC, IC, PSL, Verilog, and VHDL. VuSpec even covers new methods and best practices for the functional verification language 'e' as well as SystemC and SystemVerilog. IEEE VuSpec searches through all these standards.

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Standards

- IEEE Std 1076.1™-1999 IEEE Standard VHDL for Analog and Mixed Signal Extensions
- IEEE Std 1076.1.1™-2004 Standard for VHDL Analog and Mixed-Signal Extensions - Packages for Multiple Energy Domain Support
- IEEE Std 1076.2™-1996 (R2002) IEEE Standard VHDL Mathematical Packages
- IEEE Std 1076.3™-1997 IEEE Standard VHDL Synthesis Packages
- IEEE Std 1076.6™-2004 IEEE Standard for VHDL Register Transfer Level (RTL) Synthesis
- IEEE 1076-2005™ IEEE Standard VHDL Language Reference Manual
- IEEE Std 1164™-1993 IEEE Standard Multivalued Logic System for VHDL Model Interoperability
- IEEE Std 1364™-2005 IEEE Standard for Verilog Hardware Description Language
- IEEE Std 1364.1™-2002 IEEE Standard for Verilog® Register Transfer Level Synthesis
- IEEE Std 1481™-1999 IEEE Standard for Integrated Circuit (IC) Delay and Power Calculation System
- IEEE Std 1499™-1998 (R2004) IEEE Standard Interface for Hardware Description Models of Electronic Components
- IEEE Std 1603™-2003 IEEE Standard for an Advanced Library Format (ALF) Describing Integrated Circuit (IC)
- IEEE Std 1647™-2005, Standard for the Functional Verification Language 'e'
- IEEE Std 1666™-2005, IEEE Standard SystemC Language Reference Manual
- IEEE Std 1800™-2005 IEEE Standard for SystemVerilog: Unified Hardware Design, Specification, and Verification Language
- IEEE Std 1850™-2005, IEEE Standard for Property Specification Language (PSL)
- IEEE Std 2000.2™-1999, IEEE Recommended Practice for Information Technology - Year 2000 Test Methods

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- IEC/IEEE 61523-3-2004 IEC/IEEE Delay and power calculation standards -- Part 3: Standard Delay Format (SDF)
- IEC/IEEE 61691-1-1-2004, Behavioural Languages Part 1-1: VHDL Language Reference Manual
- IEC/IEEE 61691-4-2004, Behavioural languages-- Part 4: Verilog® Hardware Description Language
- IEC/IEEE 61691-5-2004, Behavioural languages -- Part 5: VITAL ASIC (application specific integrated circuit) Modeling Specification
- IEC IEEE 62050-2005, VHDL Register Transfer Level (RTL) Synthesis
- IEC IEEE 62142-2005, Verilog® Register Transfer Level Synthesis
- IEC 62265: 2005, Advanced Library Format (ALF) Describing Integrated Circuit (IC) Technology, Cells and Blocks

Additional Tools and Exclusive Features:

- UML and XML VHDL LRM information model (works in your web browser)
- Case Study: VHDL in Action: RASSP
- VHDL Software Tools (VGUI)
- Bonus Standard: IEEE Std 754-1985 (R1990) Binary Floating-Point Arithmetic
- Paper: A Method for VHDL Source Protection, (VHDL Encryption)
- Handbook: MIL-HDBK-62: DOCUMENTATION OF DIGITAL ELECTRONIC SYSTEMS WITH VHDL (includes change notice 1)