Semiconductor IP Quality

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TSMC

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Outline

- Why IP quality is important
- TSMC9000 Program
- IP quality standard
- Summary
The Complexity of New Processes

Design Manpower

- **IP Qualification & Sourcing**
- **Physical Design & Verification**
- **Architecture Design**
- **System Verification**

Source: IBS
The dramatic increase of complexity of SoCs has led to IP usage estimated at 80-100 IPs per 40nm/28nm SoC in the 2013/2014 timeframe.

The quality of these IPs is paramount for successful SoC products. A systematic IP quality standard is needed.
Managing Large IP Portfolio

7600+ IP titles
All major IP types
From 0.35u to 16FF+
TSMC Systems for IP Quality

TSMC developed several systems to support IP quality chain from IP registration to risk IP gating in tape-out

1) OIP website (Ecosystem partners)
   - IP registration
   - IP assessment

2) OIP internal portal (TSMC)
   - Partner management
   - IP portfolio management

3) TSMC Online (Customers)
TSMC9000™ Program

- Technically enable IP development – design collateral, training, tape-out review, information sharing, etc.
- IP development flow audit – SOP, quality control, change control ...
- IP quality assessment – physical review, design kit, simulation review
- IP Validation Center – silicon assessment, test chip audit
- IP Master – Customer tape-out consistency checks
TSMC9000 IP Quality Assessment

- Basic requirement + specific requirement by IP type

- IP quality indicator
  - QA completeness scoring by checklist, full score 100%
  - Production record, tape-out # & 8” wafer #
TSMC9000™ Hard-IP Quality Assessment

Confidence Level

Assessment Level

Volume Production
1) Customer product quantity
2) Customer product yield tracing

IP validation Center
1) Audit IP testing result by TSMC test lab

Split Lot Silicon Assessment
1) Split lot TO review
2) Silicon reports review

Typical Silicon Assessment
1) TO review
2) Silicon reports review

Pre-silicon Assessment
1) QC (design kits) review
2) Design review

DFM Compliance
1) DFM-LPE, LPC, Dummy Insertion (Mandatory for advanced tech nodes)
2) VCMP (recommended)

Physical Review
1) DRC, LVS, ERC & Antenna checks (QA)
2) IP tag
TSMC9000™ Soft-IP Quality Assessment

- RTL Code Assessment
  - RTL checks using Atrenta SpyGlass
  - QC review

- Physical Implementation Assessment (Optional)
  - DRC, LVS, ERC & Antenna checks
  - IP tag

- Volume Production IP Usage Tracking Review
  - Product quantity
  - Product yield tracing

IEEE STANDARDS ASSOCIATION
TSMC9000™ IP Validation Center

- IP Validation Center extends TSMC9000™ to audit IP testing result and post IP validation result to TSMC Online
- Any issues or failures found during IP validation must be clarified with IP partners
### Assessment Result on TSMC Online

**IP Register**
- Issue Reporting,
- Risk IP identification

**IP Tagging for wafer #**

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**TSMC9000™ IP quality assessment and acceptance**

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**IP Comparison**

<table>
<thead>
<tr>
<th>IP Name/Location</th>
<th>Technology</th>
<th>IP Category</th>
<th>IP Type</th>
<th>IP Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCH5G1G2M1P1MPHYCMH-N18LP</td>
<td>CLN40LP</td>
<td>HARD</td>
<td>Hard/ Mixed-Signal IP / PLL</td>
<td>1.1V/2.5V, This IP contains blocks which accompany the M89 MPHY v0.9 Compliant Transmitter and Receiver to ensure that they operate and meet their specifications. It broadly consists of a low jitter PLL, Bandgap Reference, LDOs and a Resilience Calibration unit.</td>
</tr>
<tr>
<td>S1P1T1N10LP</td>
<td>CLN40LP</td>
<td>HARD</td>
<td>Hard/ Mixed-Signal IP / PLL</td>
<td>1.1V/2.5V, Low Noise Programmable PLL</td>
</tr>
<tr>
<td>M11182A22L02000</td>
<td>CLN40LP</td>
<td>HARD</td>
<td>Hard/ Mixed-Signal IP / PLL</td>
<td>1.1V/2.5V, CLN40LP 1.1V/2.5V Process Dual-power 125MHz - 2GHz PLL</td>
</tr>
</tbody>
</table>

**IP Version**
- v0p1
- v1.0
- v210a

**[TSMC9000]**
- DFM Compliance: 100%
- Physical Review: 100%
- Pre-silicon Assessment: 80%
- Typical Silicon Assessment: 64%
- Split Lot Assessment: 64%

**Volume Production**
- 22/237/47
Customer can search by enter keyword of IP name, IP Partner, Technology, IP Type...

Three tool kits for better user experience
1. My Question: For customer questions tracking
2. My Favorite Search: Record search keyword to be easy for next time
3. My IPs: Pick up IP in My IPs for tracking and comparison
**TSMC IP Center – Compare and Choose**

- Tabular comparisons on the selected IP
- Contact with vendors by one click

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### IP Comparison

<table>
<thead>
<tr>
<th>IP Name</th>
<th>tcbn20socdbwp20p90</th>
<th>tcbn20socdbwp20p90cg</th>
<th>tcbn20socdbwp20p90lv</th>
<th>tcbn20socdbwp22p90lv</th>
<th>tcbn20socdbwp24p90lv</th>
</tr>
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<tbody>
<tr>
<td>Partner Name</td>
<td>tsmc</td>
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<tr>
<td>Contact Me</td>
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<tr>
<td>Geometry</td>
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<tr>
<td>Technology</td>
<td>CLN20SC</td>
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<td>IP Category</td>
<td>HARD</td>
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<td>HARD</td>
<td>HARD</td>
</tr>
<tr>
<td>IP Description</td>
<td>TSMC 20NM CMOS LOGIC SYSTEM ON CHIP SOC HKMG 0.9/1.5V, core cell library, Standard Vt, 9-track, tapeless cell layout structure, gate length 20nm, poly pitch 90nm, raw gate density = 718 Kgate/mm²</td>
<td>N205SC 9T CG std cell library</td>
<td>TSMC 20NM CMOS LOGIC SYSTEM ON CHIP SOC HKMG 0.9/1.8V, core cell library, Low Vt, 9-track, tapeless cell layout structure, gate length 20nm, poly pitch 90nm, raw gate density = 718 Kgate/mm²</td>
<td>TSMC 20NM CMOS LOGIC SYSTEM ON CHIP SOC HKMG 0.9/1.8V, core cell library, Low Vt, 9-track, tapeless cell layout structure, gate length 22nm, poly pitch 90nm, raw gate density = 718 Kgate/mm²</td>
<td>TSMC 20NM CMOS LOGIC SYSTEM ON CHIP SOC HKMG 0.9/1.8V, core cell library, Low Vt, 9-track, tapeless cell layout structure, gate length 24nm, poly pitch 90nm, raw gate density = 718 Kgate/mm²</td>
</tr>
<tr>
<td>IP Version</td>
<td>110a</td>
<td>110a</td>
<td>110a</td>
<td>110a</td>
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</tr>
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**[TSMC9000]**

| DFM Compliance | 100% | 100% | 100% | 100% | 100% |
| Physical Review | 100% | 100% | 100% | 100% | 100% |
| Pre-silicon Assessment | 100% | 100% | 100% | 100% | 100% |
| Typical Silicon Assessment | 100% | 100% | 100% | 100% | 100% |
TSMC9000 IP Tag Spec. & Utility

TSMC has defined the IP tag based on VSIA's IP tagging standard requirement and TSMC's tagging specification. As a courtesy to promote the IP tagging in the Semiconductor industry, TSMC now shares the spec. of IP tag for reference: <IP tag spec. in PDF format>

Per request, TSMC may provide TSMC9000 IP Tag Utility to IP vendors for facilitating the IP tagging tasks. Click the link to request the Utilities.

Open access via http://www.tsmc.com/english/dedicatedFoundry/services/tsmc9000_iptag.htm
Areas for IP Quality Standardization

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Summary

- TSMC continues to invest into ecosystem quality
- TSMC9000 is the TSMC ecosystem standard of IP quality
- TSMC will continue working with ecosystem partners to provide broad and high quality IP portfolio