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22 March 2007

Victor Berman
victorb@improvsys.com

Re: P1778 - Standard for Esterel v7 Language Reference Manual

Dear Victor:

I am pleased to inform you that on 22 March 2007 the IEEE-SA Standards Board approved the above referenced project until 31 December 2011. A copy of the file can be found on our website at <http://standards.ieee.org/board/nes/projects/1778.pdf>.

Now that your project has been approved, please forward a roster of participants involved in the development of this project. This request is in accordance with the IEEE-SA Operations Manual, Clause 5.1.2i under Duties of the Sponsor which states:

"Submit annually to the IEEE Standards Department an electronic roster of individuals participating on standards projects"

For your convenience, an Excel spreadsheet for your use has been posted on our website at <http://standards.ieee.org/guides/par/roster.xls>. Please forward this list to me via e-mail at s.hampton@ieee.org no later than 20 June 2007.

Please visit our website, IEEE Standards Development Online (<http://standards.ieee.org/resources/development/index.html>), for tools, forms and training to assist you in the standards development process. Also, we strongly recommend that a copy of your draft be sent to this office for review prior to the final vote by the working group to allow for a quick review by editorial staff before sponsor balloting begins.

If you should have any further questions, please contact me at +1 732 562 6003 or by email at s.hampton@ieee.org.

Sincerely,

Sherry Hampton
Administrator, Governance

Standards Activities

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PAR Request Date: 02 August 2006	
PAR Approval Date: 22 March 2007	
PAR Signature Page on File: Yes	
Type of PAR: New IEEE Standard	
Status: PAR for a New IEEE Standard	
Root Project:	
1.1 Project No.: 1778	
1.2 Type of Document: Standard	
1.3 Life Cycle: Full-Use	
1.4 Is this document in ballot now? No	
2.1 Title Standard for Esterel v7 Language Reference Manual	
3.1 Working Group Name	Esterel v7 Language Reference
Working Group Chair	Berry, Gérard Phone: +33 4 92 02 40 65 Email: Gerard.Berry@esterel-technologies.com
Working Group Vice Chair	
3.2 Sponsor	IEEE Computer Society Design Automation (C/DA)
Sponsor Chair	Berman, Victor Phone: 978-927-0555 Email: victorb@improvsys.com
Name of Standards Liaison Representative (if applicable)	
3.3 Joint Sponsor	
4.1 Type of Ballot: Individual	
4.2 Expected Date of Submission for Initial Sponsor Ballot: December 2007	
4.3 Projected Completion Date for Submittal to RevCom: June 2008	
5.1 Approximate number of people expected to work on this project: 18	
5.2 Scope: This standard is a Reference Manual for the Esterel v7 Language, which is dedicated to the specification and implementation of hardware or software reactive systems. The standard ensures unambiguous definition of the language syntax and semantics, and, therefore, full interoperability between Esterel-based software compilation, circuit synthesis, static analysis, and verification tools.	
5.3 Is the completion of this document contingent upon the completion of another document? No	

5.4 Purpose: The purpose of this standard is to provide the Electronic Design Automation, Semiconductor, Systems Design, and Software communities with a well-defined and official IEEE definition of the Esterel v7 language. Esterel v7 is not a minor variant of existing HDLs or software languages that could be defined with an addendum to existing standards. Esterel v7 is unique in its way to formally merge the kind of sequencing only found in software languages, the kind of large-scale synchronous concurrency found in hardware description languages, specific temporal control primitives that drive the life and death of activities, and full support for multiclock designs. For datapath specification, Esterel v7 supports formally defined arbitrary precision exact arithmetic, bitvectors with conversion from and to numbers according to predefined or user-defined numerical encodings, and arrays of arbitrary dimensions and types. Esterel v7 is interoperable with other standards since it can generate synthesizable HDL code (Verilog, VHDL, etc.) as well as executable software code (C, C++, SystemC, etc.).

5.5 Need for the Project: This project will provide the Electronic Design Automation, System Design, and Semiconductor communities with a formally defined language for hardware and reactive software design, verification, and implementation. Esterel sequencing, concurrency, communication, and temporal hierarchical behavior description primitives enable increased efficiency and reliability of these designs. Experience has shown that Esterel v7 designs can be 3 to 5 times smaller than HDL or C designs, while being easier to develop, verify, and communicate. The fact that equivalent hardware and software targets can be obtained from a single source increases confidence in hardware simulation by software means, and helps delaying choices between hardware and software final implementations. Furthermore, the preciseness of the semantics ensures full consistency between implementation and simulation-based or formal verification.

5.6 Stakeholders for the Standard: The stakeholders for this standard are the Electronic Design Automation industry, Semiconductor producers, and System Designers.

6.1.a. Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR prior to the PAR submittal to the IEEE-SA Standards Board? Yes Presented Date: 2007-02-05

If no, please explain:

6.1.b. Is the Sponsor aware of any copyright permissions needed for this project? No

If yes, please explain:

6.1.c. Is the Sponsor aware of possible registration activity related to this project? No

If yes, please explain:

7.1 Are there other standards or projects with a similar scope? Yes

If yes, please explain:

The scope of this project is related to but not the same as previous IEEE standards, namely the VHDL language (P1076b), the Verilog language (P1364), the SystemVerilog language (P1800), PSL (P1850)

Sponsor Organization: C/DA, CAG

Project/Standard Number: 1800, 1364, 1076, 1850

Project/Standard Date: 0000-00-00

Project/Standard Title: VHDL language (P1076b), the Verilog language (P1364), the SystemVerilog language (P1800), PSL (1850)

7.2 Is there potential for this standard (in part or in whole) to be adopted by another national, regional, or international organization? ? Do not know at this time

Technical Committee Name and Number:

Contact person:

Contact person Phone Number:

Contact person Email Address:

7.3 Will this project result in any health, safety, security, or environmental guidance that affects or applies to human health or safety? No

7.4 Additional Explanatory Notes:

8.1 Sponsor Information:

Is the Scope of this project within the approved scope/definition of the Sponsor's Charter? Yes

If no, please explain: