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09 May 2007

Rohit Kapur
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Re: P1450.6.2 - Standard for Memory Modeling in Core Test Language (CTL)

Dear Rohit:

I am pleased to inform you that on 07 May 2007 the IEEE-SA Standards Board approved the above referenced project until 31 December 2011. A copy of the file can be found on our website at <http://standards.ieee.org/board/nes/projects/1450-6-2.pdf>.

Now that your project has been approved, please forward a roster of participants involved in the development of this project. This request is in accordance with the IEEE-SA Operations Manual, Clause 5.1.2i under Duties of the Sponsor which states:

"Submit annually to the IEEE Standards Department an electronic roster of individuals participating on standards projects"

For your convenience, an Excel spreadsheet for your use has been posted on our website at <http://standards.ieee.org/guides/par/roster.xls>. Please forward this list to me via e-mail at s.hampton@ieee.org no later than 05 August 2007.

Please visit our website, IEEE Standards Development Online (<http://standards.ieee.org/resources/development/index.html>), for tools, forms and training to assist you in the standards development process. Also, we strongly recommend that a copy of your draft be sent to this office for review prior to the final vote by the working group to allow for a quick review by editorial staff before sponsor balloting begins.

If you should have any further questions, please contact me at +1 732 562 6003 or by email at s.hampton@ieee.org.

Sincerely,

Sherry Hampton
Administrator, Governance
Standards Activities
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PAR Request Date: 16 March 2007**PAR Approval Date:** 07 May 2007**PAR Signature Page on File:** Yes**Type of PAR:** New IEEE Standard**Status:** PAR for a New IEEE Standard**Root Project:****1.1 Project No.:** **1450.6.2****1.2 Type of Document:** Standard**1.3 Life Cycle:** Full-Use**1.4 Is this document in ballot now?** No**2.1 Title**

Standard for Memory Modeling in Core Test Language (CTL)

3.1 Working Group Name [Working Group for Core Test Language \(CTL\)](#)**Working Group Chair**
[Adham, Saman](#)
Phone: 613-722-2051 X242
Email: saman@ieee.org**Working Group Vice Chair**
[Kapur, Rohit](#)
Phone: 650-584-1487
Email: rkapur@synopsys.com**3.2 Sponsor** [IEEE Computer Society Test Technology \(C/TT\)](#)**Sponsor Chair**
[Kapur, Rohit](#)
Phone: 650-584-1487
Email: rkapur@synopsys.com**Name of Standards Liaison Representative (if applicable)****3.3 Joint Sponsor****4.1 Type of Ballot:** Individual**4.2 Expected Date of Submission for Initial Sponsor Ballot:** November 2008**4.3 Projected Completion Date for Submittal to RevCom:** November 2009**5.1 Approximate number of people expected to work on this project:** 25

5.2 Scope: System on Chip (SoC) test requires reuse of test data and test structures developed for individual cores (designs) when integrated into larger integrated circuits. This activity defines language constructs sufficient to represent the context of a memory-core and of the integration of that memory-core into an SoC, to facilitate development and reuse of test and repair mechanisms for memories. This activity also defines constructs that represent the test structures internal to the memory-core for reuse in the creation of the tests for the logic outside the memory-core. Semantic rules are defined for the language to facilitate interoperability between different entities (the memory-core provider, the system integrator, and the automation tool developer) involved in the creation of an SoC. The capabilities are an extension of IEEE 1450.6-2005. As a result of this extension, CTL's limitations of handling memories are addressed.

5.3 Is the completion of this document contingent upon the completion of another document? No

5.4 Purpose: To develop an extension to the CTL language that provides a sufficient description of a memory-core to support the development and reuse of test and repair mechanisms for that memory after integration into SoC environment and enable creation of test patterns for the logic on the SoC external to the memory.

5.5 Need for the Project: The existing CTL standard does not address all memory specific characteristics and structural information required to create memory test patterns and sequences.

5.6 Stakeholders for the Standard: The stakeholders for this project are: electronic design automation industry, telecom industry, medical industry, memory design and manufacturing industry, Instrumentation industry, automobile industry, manufacturing automation, and any industry that requires electronic integrated circuit.

6.1.a. Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR prior to the PAR submittal to the IEEE-SA Standards Board? Yes Presented Date: 2006-05-23

If no, please explain:

6.1.b. Is the Sponsor aware of any copyright permissions needed for this project? No

If yes, please explain:

6.1.c. Is the Sponsor aware of possible registration activity related to this project? No

If yes, please explain:

7.1 Are there other standards or projects with a similar scope? No

If yes, please explain:

Sponsor Organization:

Project/Standard Number:

Project/Standard Date: 0000-00-00

Project/Standard Title:

7.2 Is there potential for this standard (in part or in whole) to be adopted by another national, regional, or international organization? ? Do not know at this time

Technical Committee Name and Number:

Contact person:

Contact person Phone Number:

Contact person Email Address:

7.3 Will this project result in any health, safety, security, or environmental guidance that affects or applies to human health or safety? No

7.4 Additional Explanatory Notes:

8.1 Sponsor Information:

Is the Scope of this project within the approved scope/definition of the Sponsor's Charter? Yes

If no, please explain: