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12 August 2004

Peter Ashenden  
Ashenden Designs Pty Ltd  
P.O. Box 640  
Stirling SA 5152  
AUSTRALIA  
peter@ashenden.com.au

Re: P1364 - Verilog Hardware Description Language

Dear Peter:

I am pleased to inform you that on 12 August 2004 the IEEE-SA Standards Board approved the above referenced project until 31 December 2007. A copy of the file can be found on our website at <http://standards.ieee.org/board/nes/projects/1364.pdf>.

Now that your project has been approved, please forward a roster of participants involved in the development of this project. This request is in accordance with the IEEE-SA Operations Manual, Clause 5.1.2i under Duties of the Sponsor which states:

"Submit annually to the IEEE Standards Department an electronic roster of individuals participating on standards projects"

For your convenience, an Excel spreadsheet for your use has been posted on our website at <http://standards.ieee.org/guides/par/roster.xls>. Please forward this list to me via e-mail at [j.haasz@ieee.org](mailto:j.haasz@ieee.org) no later than 9 November 2004.

Please visit our website, IEEE Standards Development Online (<http://standards.ieee.org/resources/development/index.html>), for tools, forms and training to assist you in the standards development process. Also, we strongly recommend that a copy of your draft be sent to this office for review prior to the final vote by the working group to allow for a quick review by editorial staff before sponsor balloting begins.

If you should have any further questions, please contact me at 732-562-6367 or by email at [j.haasz@ieee.org](mailto:j.haasz@ieee.org).

Sincerely,

Jodi Haasz  
Program Manager  
International Stds Programs and Governance  
Standards Activities  
Phone +1 732 562 6367  
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Email: [j.haasz@ieee.org](mailto:j.haasz@ieee.org)

cc: [johny.srouji@intel.com](mailto:johny.srouji@intel.com)

# PAR FORM

**PAR Status:** Revision of Revision PAR

**PAR Approval Date:** 2004-08-12

**PAR Signature Page on File:** Yes

**1. Assigned Project Number:** 1364

**2. Sponsor Date of Request:** 2004-07-06

**3. Type of Document:** Standard for

**4. Title of Document:**

**Draft:** Verilog Hardware Description Language

**5. Life Cycle:** Full-Use

**6. Type of Project:**

**6a. Is this an update to an existing PAR?** Yes

**If Yes: Indicated PAR number/approval date:** 1364 - 2003-03-20

**If Yes: Is this Project in Ballot now?** No

**6b. The Project is a:** Revision of Std 1364-2001

**7. Working Group Information:**

**Name of Working Group:** SystemVerilog Working Group

**Approximate Number of Expected Working Group Members:**10

**8. Contact information for Working Group Chair:**

**Name of Working Group Chair:** Johny Srouji

**Telephone:** 972-4-8655265 **FAX:** 972-4-8655265

**Email:** johny.srouji@intel.com

**9. Contact information for Co-Chair/Official Reporter, Project Editor or Document Custodian if different from the Working Group Chair:**

**Name of Co-Chair/Official Reporter, Project Editor or Document Custodian:**

**Telephone: FAX:**

**Email:**

**10. Contact information for Sponsoring Society or Standards Coordinating Committee:**

**Name of Sponsoring Society and Committee:** Computer Society Design Automation

**Name of Sponsoring Committee Chair:** Peter Ashenden

**Telephone:** +61883397532 **FAX:** +61883392616

**Email:** peter@ashenden.com.au

**Name of Liaison Rep. (if different from the Sponsor Chair):**

**Telephone: FAX:**

**Email:**

**Name of Co-Sponsoring Society and Committee:**

**Name of Co-Sponsoring Committee Chair:**

**Telephone: FAX:**

**Email:**

**Name of Liaison Rep. (if different from the Sponsor Chair):**

**Telephone: FAX:**

**Email:**

**11. The Type of ballot is:** Entity Sponsor Ballot

**Expected Date of Submission for Initial Sponsor Ballot:** 2005-03-30

**12. Fill in Projected Completion Date for Submittal to RevCom:** 2005-09-30

**Explanation for Modified PAR that completion date is being extended past the original four-year life of the PAR:**

**13. Scope of Proposed Project:**

Verilog is a Hardware Description Language which was standardized as IEEE-1364-1995, and revised as 1364-2001. The proposed project will revise Verilog 1364 to correct and clarify features ambiguously or erroneously described in the 1364-1995 and 1364-2001 revisions and to resolve incompatibilities and inconsistencies of the existing IEEE 1364-2001 requirements with the proposed enhancements in P1800.

**Is the completion of this document contingent upon the completion of another document?** No

**14. Purpose of Proposed Project:**

The purpose of the original document, IEEE Std 1364-2001, was to provide an industry standard based on the Verilog Hardware Description Language. The reason for the document's revision is to incorporate corrections that have been identified by the working group since 1364-1995 and 1364-2001 were published by the IEEE.

**14a. Reason for the standardization project:**

The purpose of this project is to provide a standard that complements IEEE 1076-IEEE Standard VHDL Language Reference Manual from the register transfer level downward, by providing an industry standard based on the Verilog Hardware Description Language, as well as incorporating corrections that have been identified by the working group since the 1364-1995 and 1364-2001 were published by the IEEE. The language is currently used by integrated circuit designers to specify their designs at the switch, gate and RTL levels. Correction of ambiguities and minor technical errors will ensure greater interoperability between tools that implement the language, and will provide a sounder basis for the proposed enhancements in P1800.

**15. Intellectual Property:**

**Has the sponsor reviewed the IEEE patent policy with the working group?** Yes

**Is the sponsor aware of copyrights relevant to this project?** No

**Is the sponsor aware of trademarks relevant to this project?** No

**Is the sponsor aware of possible registration of objects or numbers due to this project?** No

**16. Are there other documents or projects with a similar scope?** Yes

IEEE 1076-IEEE Standard VHDL Language Reference Manual

**Similar Scope Project Information:**

SimSponsor: IEEE C/DA SimProjNo: P1076 SimProjD: 2003-02-13 SimTitle: Standard VHDL Language Reference Manual -- Simulation Run-Time Application Interface

**17. Is there potential for this document (in part or in whole) to be adopted by another national , regional or international organization?** Yes

**If yes, please answer the following questions:**

**Which International Organization/Committee?** IEC TC93 WG2

**International Contact Information?** Alex N Zamfirescu  
ASC  
644 Emerson St., Suite 10  
Palo Alto, CA 94301  
650-323-4643  
650-323-4643  
a.zamfirescu@ieee.org

**18. If the project will result in any health, safety, or environmental guidance that affects or applies to human health or**

**safety, please explain in five sentences or less.**

**19. Additional Explanatory Notes: (Item Number and Explanation)**

Item 6: DASC-SC resolved to request modification of the PAR so that Verilog and SystemVerilog (P1800) can be administered together, leverage each language strength and eventually be unified by one working group.