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31 March 2006

Chuck Adams  
IBM  
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Re: P1149.7 - Standard for Reduced-pin and Enhanced-functionality Test Access Port and Boundary Scan Architecture

Dear Chuck:

I am pleased to inform you that on 30 March 2006 the IEEE-SA Standards Board approved the above referenced project until 31 December 2010. A copy of the file can be found on our website at <http://standards.ieee.org/board/nes/projects/1149-7.pdf>.

Now that your project has been approved, please forward a roster of participants involved in the development of this project. This request is in accordance with the IEEE-SA Operations Manual, Clause 5.1.2i under Duties of the Sponsor which states:

"Submit annually to the IEEE Standards Department an electronic roster of individuals participating on standards projects"

For your convenience, an Excel spreadsheet for your use has been posted on our website at <http://standards.ieee.org/guides/par/roster.xls>. Please forward this list to me via e-mail at [j.haasz@ieee.org](mailto:j.haasz@ieee.org) no later than 28 June 2006.

Please visit our website, IEEE Standards Development Online (<http://standards.ieee.org/resources/development/index.html>), for tools, forms and training to assist you in the standards development process. Also, we strongly recommend that a copy of your draft be sent to this office for review prior to the final vote by the working group to allow for a quick review by editorial staff before sponsor balloting begins.

If you should have any further questions, please contact me at 732-562-6367 or by email at [j.haasz@ieee.org](mailto:j.haasz@ieee.org).

Sincerely,

Jodi Haasz  
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# PAR FORM

**PAR Status:** New PAR

**PAR Approval Date:** 30 March 2006

**PAR Signature Page on File:** Yes

**1. Assigned Project Number:** P1149.7

**2. Sponsor Date of Request:** 2006-02-02

**3. Type of Document:** Standard for

**4. Title of Document:**

**Draft:** Standard for Reduced-pin and Enhanced-functionality Test Access Port and Boundary Scan Architecture

**5. Life Cycle:** Full-Use

**6. Type of Project:**

**6a. Is this an update to an existing PAR?** No

**6b. The Project is a:** New Standard

**7. Working Group Information:**

**Name of Working Group:** P1149.7 Working Group

**Approximate Number of Expected Working Group Members:**15

**8. Contact information for Working Group Chair:**

**Name of Working Group Chair:** Tom Vial

**Telephone:** +33 4 93 22 15 81 **FAX:**

**Email:** t-vial@ti.com

**9. Contact information for Co-Chair/Official Reporter, Project Editor or Document Custodian if different from the Working Group Chair:**

**Name of Co-Chair/Official Reporter, Project Editor or Document Custodian:**

**Telephone:** **FAX:**

**Email:**

**10. Contact information for Sponsoring Society or Standards Coordinating Committee:**

**Name of Sponsoring Society and Committee:** IEEE-SA Board of Governors Corporate Advisory Group

**Name of Sponsoring Committee Chair:** Chuck Adams

**Telephone:** 914-765-4382 **FAX:** 914-765-4420

**Email:** wcadams@us.ibm.com

**Name of Liaison Rep. (if different from the Sponsor Chair):**

**Telephone:** **FAX:**

**Email:**

**Name of Co-Sponsoring Society and Committee:** IEEE Computer Society Test Technology

**Name of Co-Sponsoring Committee Chair:** Rohit Kapur

**Telephone:** 650-584-1487 **FAX:** 650-584-4128

**Email:** rkapur@synopsys.com

**Name of Liaison Rep. (if different from the Sponsor Chair):**

**Telephone:** **FAX:**

**Email:**

**11. The Type of ballot is:** Entity Sponsor Ballot

**Expected Date of Submission for Initial Sponsor Ballot:** December 2006

**12. Projected Completion Date for Submittal to RevCom:** October 2007

**Target Extension Request Information for a Modified PAR whose completion date is being extended past the original four-year life of the PAR:**

**13. Scope of Proposed Project:**

The standard will define a link between IEEE Std 1149.1 - 2001, IEEE Standard Test Access Port and Boundary Scan Architecture interfaces in Debug and Test Systems (DTS) and IEEE 1149.1 (JTAG) interfaces in Target Systems (TS). The link defined by this standard introduces an additional layer between these legacy interfaces. This layer may be viewed as an adapter that provides new functionality and features while preserving all elements of the original IEEE 1149.1 (JTAG) interfaces. The standard will define the link behavior (including timing characteristics of signals), protocols, and functionality of the adapters deployed within the DTS and TS. The standard will not modify or create inconsistencies with IEEE 1149.1 (JTAG). The standard will define a superset of the IEEE 1149.1 specification and achieve compliance with the IEEE 1149.1 standard.

**Is the completion of this document contingent upon the completion of another document?** No

**14. Purpose of Proposed Project:**

The purpose of the standard is to define a debug and test interface which meets an expanding set of challenges facing debug and test systems (many which have emerged since the inception of the original IEEE 1149.1) while preserving the hardware and software investments of the many industries currently using IEEE 1149.1.

**15. Reason for the Proposed Project:**

Increased integration levels, the consolidation of systems into fewer chips, and the increased focus on low-power operation and single-chip system solutions have created testing and debugging challenges that did not exist when the IEEE Std 1149.1 standard was developed. Some of the problems facing the industry include:

- Expanding interconnect requirements and shrinking die sizes have produced severe pressure to reduce pins allocated for any given purpose.
- Expanding system complexity is driving higher and higher expectations for the performance and functionality of debug, test and trace systems.
- Sophisticated power management techniques, both at PCB level and systems-on-a-chip (SOC), face increasing obstacles from IEEE Std 1149.1 which did not anticipate these requirements.
- Broad deployment of IP cores using different debug/test methodologies are increasingly difficult to support with a single, standard external debug and test interface.
- Extraordinarily broad adoption of IEEE Std 1149.1 has produced an environment intolerant of discontinuities in debug and test systems, inhibiting the introduction of new technologies.

The goal of this project is to enable existing IEEE Std 1149.1-based systems to be easily upgraded to meet these challenges without creating discontinuities with legacy systems. The benefits of this standard include:

- Minimizing the number of IC pins used for debugging and test communication
- Expanding functionality and performance of debug and test systems:
  - o Supports multiple configurations (Series, Star, 2-pin, 4-pin)
  - o Supports glueless multi-device communications with these configurations
  - o Increases port bandwidth for instrumentation data during low-bandwidth IEEE Std 1149.1 transactions.
  - o supports specialized debug additions via custom protocol extensions
  - o provides background data transfers concurrent with advanced scan transactions
- Supporting requirements of highly power-managed systems:
  - o Adapts to the power-conscious attributes of the systems it is intended to support
  - o Accommodates slow system response such as power-saving modes or component clock limitations
  - o Comprehends board power domains and synchronized operations across multiple debug ports
  - o Supports operating frequencies from DC to 100 MHz
- Providing debug access that is independent of CPU and debug technology
  - o backwards compatible with pre-existing silicon-on-chip (SOC) intellectual property (IP)
- Avoiding discontinuities in the DTS software, DTS hardware, and TS silicon through compatibility with the existing IEEE Std 1149.1 interface and all standard IEEE Std 1149.1 hardware/software:
  - o Preserves investment: adding a IEEE Std 1149.7 adapter to legacy DTS equipment enables use with IEEE Std 1149.7 systems
  - o Enables seamless transition: can support full capability of each component in systems mixing IEEE Std 1149.1/IEEE Std 1149.7 devices or tools.

In addition to these technical benefits, the project meets important criteria for successful standards. It meets user expectations of “as good or better” by reproducing existing IEEE Std 1149.1 capabilities (nothing is lost). It stands to reason that providing an upgrade path to the huge installed base of IEEE Std 1149.1 will accelerate the adoption of a new standard much faster than any other approach, and will do so without creating conflict or disturbance for the IEEE Std 1149.1 standard. Stakeholders include semiconductor manufacturers, debug and test system manufacturers, system designers, and OEMs in nearly every segment of the electronics market (especially consumer electronics and mobile communications).

**16. Intellectual Property:**

- a. **Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR?** No 0000-00-00  
The policy will be presented to the Working Group at their first meeting.
- b. **Is the sponsor aware of copyright permissions needed for this project?** Yes  
This project is based on a draft specification from Texas Instruments.
- c. **Is the sponsor aware of trademarks that apply to this project?** No
- d. **Is the sponsor aware of possible registration activity related to this project?** No

**17. Are there other documents or projects with a similar scope?** No**Similar Scope Project Information:****18. Is there potential for this document (in part or in whole) to be adopted by another national , regional or international organization?** Do not know at this time

If yes, the following questions must be answered:

**Organization Name?**

**Technical**

**Committee**

**International**

**Contact**

**Information?**

**19. Will this project result in any health, safety, or environmental guidance that affects or applies to human health or safety?** No

If yes, please explain:

**20. Sponsor Information**

- a. **Is the scope of this project within the approved/scope/definition of the Sponsor's Charter?** Yes

If no, please explain:

- b. **The Sponsor's procedures have been accepted by the IEEE-SA Standards Board Audit Committee?** Yes

**21. Additional Explanatory Notes: (Item Number and Explanation)**

I have entered myself (Tom Vial) as the chairperson only temporarily, while I work to prepare initial drafts of this PAR. Another individual from Texas Instruments will be identified before this PAR is finalized and submitted. Texas Instruments is now applying for corporate membership. Please note that this is the first project that has been submitted with the IEEE-ISTO (MIPI).