Sherry Hampton/STDS/STAFF/US/IEEE
07/21/2006 12:00 PM

To wcadams@us.ibm.com
cc vberman@cadence.com, srouji@us.ibm.com
bcc
Subject Approval of Project - P1800

31 July 2006

Chuck Adams
IBM
North Castle Drive
Armonk, NY 10504
wcadams@us.ibm.com

Re: P1800 - Standard for SystemVerilog: Unified Hardware Design, Specification and Verification Language

Dear Chuck:

I am pleased to inform you that on 28 July 2006 the IEEE-SA Standards Board approved the above referenced project until December 2010. NesCom strongly encourages the working group to update the scope and purpose on the PAR. The scope and purpose on the PAR should be as close as possible to the scope and purpose that will appear in the approved standard. The working group should submit a modified PAR when these updates are prepared.

A copy of the file can be found on our website at http://standards.ieee.org/board/nes/projects/1800.pdf.

Now that your project has been approved, please forward a roster of participants involved in the development of this project. This request is in accordance with the IEEE-SA Operations Manual, Clause 5.1.2i under Duties of the Sponsor which states:

"Submit annually to the IEEE Standards Department an electronic roster of individuals participating on standards projects"

For your convenience, an Excel spreadsheet for your use has been posted on our website at http://standards.ieee.org/guides/par/roster.xls. Please forward this list to me via e-mail at s.hampton@ieee.org no later than 26 October 2006.

Please visit our website, IEEE Standards Development Online (http://standards.ieee.org/resources/development/index.html), for tools, forms and training to assist you in the standards development process. Specifically for entity projects, please be aware that baseline entity sponsor procedures (http://standards.ieee.org/corpforum/cag/sponsor.html) and entity working group procedures (http://standards.ieee.org/corpforum/cag/wgproc.html) are available for your use. Guides to

the policies and procedures of entity standardization can be found at http://standards.ieee.org/corpforum/participation/corpstdspandp.html.

You should also be aware that anyone who wishes to earn and maintain voting rights in an entity working group must pay an annual entity project participation fee. An initial roster of contacts who have indicated an interest in becoming a voting member of the working group and who therefore should be invoiced for this fee should be submitted to Lauren Wright at the IEEE at the address on this letter or to l.wright@ieee.org no later than two weeks from the date of this letter.

If you have any questions about the rules of entity project development, please contact Mary Lynne Nielsen at m.nielsen@ieee.org.

Also, we strongly recommend that a copy of your draft be sent to this office for review prior to the final vote by the working group to allow for a quick review by editorial staff before sponsor balloting begins.

If you should have any further questions, please contact me at +1 732 562 6003 or by email at s.hampton@ieee.org.

Sincerely,

Sherry Hampton
Administrator, Governance
Standards Activities
Phone +1 732 562 6003
FAX +1 732 875 0695
Email: s.hampton@ieee.org

PAR Request Date: 09 June 2006

PAR Approval Date: 28 July 2006

PAR Signature Page on File: Yes

Type of Project: Revision to IEEE Standard

Status: Revision to an Existing IEEE Std 1800-2005

Root Project:

1.1 Project No.: **P1800**

1.2 Type of Document: Standard

1.3 Life Cycle: Full-Use

1.4 Is this document in ballot now? No

2.1 Title	**Old Title**
Standard for SystemVerilog: Unified Hardware Design, Specification and Verification Language	IEEE Standard for SystemVerilog: Unified Hardware Design, Specification and Verification Language

2.1 Amendment/Corrigenda Title

3.1 Working Group Name	SystemVerilog Language Working Group
Working Group Chair	Srouji, Johny Phone: 512-838-0252 Email: srouji@us.ibm.com
Working Group Vice Chair	
3.2 Sponsor	IEEE-SA Board of Governors Corporate Advisory Group (BOG/CAG)
Sponsor Chair	Adams, Chuck Phone: 914-765-4382 Email: wcadams@us.ibm.com
Name of Standards Liaison Representative (if applicable)	
3.3 Joint Sponsor	IEEE Computer Society Design Automation (C/DA) Berman, Victor Phone: 978-262-6560 Email: vberman@cadence.com

4.1 Type of Ballot: Entity

4.2 Expected Date of Submission for Initial Sponsor Ballot: June 2008

4.3 Projected Completion Date for Submittal to RevCom: December 2008

5.1 Approximate number of people expected to work on this project: 10

5.2 Scope: SystemVerilog 1800 is a Unified Hardware Design, Specification and Verification language. Verilog 1364-2005 is a design language. Both standards were approved by the IEEE-SASB in November 2005. This standard creates new revisions of the Verilog 1364 and SystemVerilog 1800 IEEE standards, which include Errata fixes and resolutions; enhancements; Enhanced assertion language; Merge of Verilog LRM and SystemVerilog 1800 LRM into a single LRM; Integration with AMS; and insures interoperability with other languages such as SystemC and VHDL.	**Old Scope:** SystemVerilog is a Unified Hardware Design, Specification and Verification language that is based on the work done by Accellera, a consortium of Electronic Design Automation (EDA), semiconductor, and system companies. The proposed project will create an IEEE standard that is leveraged from Accellera SystemVerilog 3.1a. The new standard will include design specification methods, embedded assertions language, test bench language including coverage and assertions API, and a direct programming interface. The proposed SystemVerilog standard enables a productivity boost in design and validation, and covers design, simulation, validation, and formal assertion based verification flows.
5.3 Is the completion of this document contingent upon the completion of another document? No	
5.4 Purpose: The purpose of this project is to provide the EDA, Semiconductor, and System Design communities with a solid and well-defined IEEE Unified Hardware Design, Specification and Verification standard language, while resolving Errata and developing enhancements to current SystemVerilog 1800 IEEE standard. The language is designed to co-exist, be interoperable, possibly merge, and enhance those hardware description languages presently used by designers.	**Old Purpose:** The purpose of this project is to provide the EDA, Semiconductor, and System Design communities with a well-defined and official IEEE Unified Hardware Design, Specification and Verification standard language. The language is designed to co-exist and enhance those hardware description languages presently used by designers while providing the capabilities lacking in those languages.
5.5 Need for the Project: With the ever increasing complexity of Very Large Scale Integrated Circuit design (VLSI) in the industry as driven by performance, functionality and power tradeoffs, the requirements for an enhanced, more powerful and extensive design language is also increasing. New designs include deeper pipelines, increased logic functionality, complexity, and power issues as well as explosion in the number of lines of Register Transfer Level (RTL) code as a result of low abstraction level of the design supported by the existing languages. This has caused an increase, not only in design complexity, but also in the verification problem. Verification efforts are consuming 60% of the total design cycle and verification gets more challenging when multiple disciplines are used at different stages of the design. Examples of these disciplines are, design specification, assertion based design, test bench based validation, coverage based specifications, and more. SystemVerilog 1800 was developed to enable the use of a unified language for abstract and detailed specification of the design, specification of assertions, coverage, and test bench verification that is based on manual or automatic methodologies. It also offers Application Programming Interfaces (API's) for coverage and assertions, a vendor independent API to access proprietary waveform file formats, and a direct programming interface to access proprietary functionality. This standardization project will further develop the current IEEE standard for SystemVerilog in order to meet the increasing usage of the language as well as enabling consistent tool behavior from different vendors. The new revision of the standard will include resolutions and clarifications to Errata and critical enhancements that will enable successful usage of the hardware design and verification language. Furthermore, and as SystemVerilog is a superset of Verilog, the new revision will merge with Verilog 1364-2005 standard to ensure a single reference manual for users and EDA vendors alike. The new standard will also enable interoperability with existing languages such as VHDL and SystemC, as well as integration with Analog Mixed Signal (AMS).	
5.6 Stakeholders for the Standard: VLSI design engineers and the EDA industry.	
6.1.a. Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR prior to the PAR submittal to the IEEE-SA Standards Board? Yes **Presented Date:** 2006-05-09 If no, please explain: The policy has been reviewed at every meeting of the Study Group and will be reviewed at all Working Group meetings the first of which will be held after approval of the PAR.	
6.1.b. Is the Sponsor aware of any copyright permissions needed for this project? No If yes, please explain:	
6.1.c. Is the Sponsor aware of possible registration activity related to this project? No If yes, please explain:	

7.1 Are there other standards or projects with a similar scope? Yes
If yes, please explain:
The scope of this PAR covers portions of the scope of previous PARs submitted by IEEE CS DASC. The existing PARs are: 1076b, 1647 and 1666. The purpose of this PAR clearly states the intent to co-exist with the results of the standards produced by these Working Groups; to the best of our knowledge there are no impediments at this time to achieve the goal. In addition Accellera and OSCI (Open SystemC Initiative), both industry consortia within the EDA industry, have done work that covers the area of the scope of this PAR. OSCI with SystemC (a system design language) and Accellera with PSL and OVL, both assertion languages used in the verification of electronic circuit designs.
Sponsor Organization: IEEE CAG & DASC
Project/Standard Number: 1076b, 1647, 1666, 1850
Project/Standard Date: 2007-06-01
Project/Standard Title: IEEE Standard for VHDL, IEEE Standard for 'e' Language, IEEE Standard for SystemC, Accellera Standard for Open Verification Library, IEEE Standard Property Specification Language

7.2 Is there potential for this standard (in part or in whole) to be adopted by another national, regional, or international organization? ? Yes
Technical Committee Name and Number: IEC TC93 WG2
Contact person: John Messina
Contact person Phone Number: +1 301 975 4284
Contact person Email Address: john.messina@nist.gov

7.3 Will this project result in any health, safety, security, or environmental guidance that affects or applies to human health or safety? No

7.4 Additional Explanatory Notes:

8.1 Sponsor Information:
Is the Scope of this project within the approved scope/definition of the Sponsor's Charter? Yes
If no, please explain: