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07 June 2007

Rohit Kapur
Synopsys Inc.
700 East Middlefield Road
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Re: P1581 - Standard for Static Component Interconnection Test Protocol and Architecture

Dear Rohit:

I am pleased to inform you that on 07 June 2007 the IEEE-SA Standards Board approved the above referenced project until 31 December 2007. A copy of the file can be found on our website at <http://standards.ieee.org/board/nes/projects/1581.pdf>.

Now that your project has been approved, please forward a roster of participants involved in the development of this project. This request is in accordance with the IEEE-SA Operations Manual, Clause 5.1.2i under Duties of the Sponsor which states:

"Submit annually to the IEEE Standards Department an electronic roster of individuals participating on standards projects"

For your convenience, an Excel spreadsheet for your use has been posted on our website at <http://standards.ieee.org/guides/par/roster.xls>. Please forward this list to me via e-mail at s.hampton@ieee.org no later than 05 September 2007.

Please visit our website, IEEE Standards Development Online (<http://standards.ieee.org/resources/development/index.html>), for tools, forms and training to assist you in the standards development process. Also, we strongly recommend that a copy of your draft be sent to this office for review prior to the final vote by the working group to allow for a quick review by editorial staff before sponsor balloting begins.

If you should have any further questions, please contact me at +1 732 562 6003 or by email at s.hampton@ieee.org.

Sincerely,

Sherry Hampton
Administrator, Governance
Standards Activities
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PAR Request Date: 26 April 2007**PAR Approval Date:** 07 June 2007**PAR Signature Page on File:** Yes**Type of PAR:** Modification to Approved PAR**Status:** Modification to a Previously Approved PAR P1581, 21 February 2001**Root Project:** New Project**1.1 Project No.:** **1581****1.2 Type of Document:** Standard**1.3 Life Cycle:** Full-Use**1.4 Is this document in ballot now?** No**2.1 Title**

Standard for Static Component Interconnection Test Protocol and Architecture

3.1 Working Group Name[Static Component Interconnection Test Protocol and Architecture Working Group](#)**Working Group Chair**[Ehrenberg, Heiko](#)

Phone: 512-502-3010

Email: h.ehrenberg@goepel.com

Working Group Vice Chair[Russell, Robert J](#)

Phone: 1-617-269-3768

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3.2 Sponsor[IEEE Computer Society Test Technology \(C/TT\)](#)**Sponsor Chair**[Kapur, Rohit](#)

Phone: 650-584-1487

Email: rkapur@synopsys.com

Name of Standards Liaison Representative (if applicable)**3.3 Joint Sponsor****4.1 Type of Ballot:** Individual**4.2 Expected Date of Submission for Initial Sponsor Ballot:** June 2008**4.3 Projected Completion Date for Submittal to RevCom:** March 2009**5.1 Approximate number of people expected to work on this project:** 15

5.2 Scope: This standard defines a low-cost method for testing the interconnection of discrete, complex memory Integrated Circuits (ICs) where additional pins for testing are not available and implementing boundary scan (IEEE 1149.1) is not feasible. This standard describes the implementation rules for the test logic and test mode access/exit methods in compliant ICs. The standard is limited to the behavioral description of the implementation and will not include the technical design for the test logic or test mode control circuitry.

Old Scope: This project will develop a standard protocol for testing the interconnection of low-cost complex memory ICs where additional pins for testing are not available and implementing boundary scan (IEEE 1149.1) is not feasible. This protocol will describe the implementation rules for the SCITT test logic in ICs which is needed for testing and describes test mode access/exit. The project is limited to the behavioral description of the implementation and will not include the technical design for the test.

5.3 Is the completion of this document contingent upon the completion of another document? No

5.4 Purpose: There is currently no defined, independent standard for test technology in memory devices. Each vendor is free in the way of implementing test hardware functionality in their Integrated Circuits (ICs) to support connectivity tests. Without an independent standard, testability is reduced and test coverage may not be complete - making the test technology less useful for others. This standard will improve interconnect test for discrete memory devices by specifying implementation rules for test logic and test mode access/exit methods included in memory ICs as guidance both to IC vendors implementing the standard, and to test equipment manufacturers supporting this standard. The standard is aimed at ICs that are otherwise not provisioned with Design For Testability (DFT) for any reason, targeting primarily memory devices but also allowing for implementation in other devices, while supporting the highest fault coverage and pin level diagnostics of board level connectivity faults on such devices.

Old Purpose: There is currently no defined, independent standard for this new test technology. Each vendor is free in the way of implementing test hardware functionality in their ICs. Without an independent standard, testability is reduced and test coverage may not be complete - making the test technology less useful for others. This Standard will provide the specification of the protocol and implementation rules for the highest fault coverage and diagnosis. This Standard will also provide a specification for test mode access/exit, provide guidance to both IC vendors, implementing the standard, and test manufacturers to support this standard. The standard also allows for implementation in devices other than memories. In contrast to IEEE 1149.1 standard this standard provides a static test method, requires less pins and is lower in cost.

5.5 Need for the Project: Many IC's, in particular memory devices become more complex with every generation, yet they do not provide any DFT features to support connectivity tests at board and system level. IEEE 1149.1 is well established in highly complex digital IC's, yet especially memory device vendors are hesitant to implement this technology in their devices. Boundary Scan based memory cluster tests are the state of the art today, although modern memory device interfaces routinely inhibit the application of such tests. And if Boundary Scan based memory cluster tests are possible, they often take a relatively long time to execute and their diagnostic resolution may be limited. There is a need for a standardized interconnect test technology in memory devices. Such a standard would vastly improve the support of connectivity tests in memory devices that do not implement IEEE 1149.1 for whatever reason, resulting in improved testability and diagnostics.

5.6 Stakeholders for the Standard: Stakeholders are individuals and organizations involved in design, manufacturing, and test of integrated circuits (especially any kind of Memory Devices that do not implement test resources as defined in IEEE 1149.1) and higher-level electronic assemblies across a broad range of end-equipment segments, including, but not limited to, aerospace, automotive, computing, consumer electronics, medical, and telecommunications, and their supply chains, including, but not limited to, electronic design automation and test equipment.

6.1.a. Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR prior to the PAR submittal to the IEEE-SA Standards Board? Yes Presented Date: 2007-05-15

If no, please explain: IEEE-SA policy on Intellectual Property has been presented at P1581 working group meetings in previous years. The membership of the working group has not been changing much, however, to remind all members of the policy, the material on Intellectual Property will be presented again at the beginning of the next working group meeting on May 15, 2007.

6.1.b. Is the Sponsor aware of any copyright permissions needed for this project? No

If yes, please explain:

6.1.c. Is the Sponsor aware of possible registration activity related to this project? No

If yes, please explain:

7.1 Are there other standards or projects with a similar scope? Yes

If yes, please explain:

The IEEE 1149.1 "standard Test Access Port and Boundary Scan Architecture" is a standard which describes a test methodology for ICs where boundary scan is incorporated and accessed through a standard port. This proposed standard (P1581) incorporates a test technology for ICs (Memories) in which it is not possible or commercially unwanted to implement Boundary Scan. This proposed standard is complementary to the currently existing standard (IEEE 1149.1) and increases the amount of testability on printed circuit boards.

Sponsor Organization: IEEE C/TT

Project/Standard Number: 1149.1

Project/Standard Date: 2001-07-23

Project/Standard Title: IEEE Standard Test Access Port and Boundary Scan Architecture

7.2 Is there potential for this standard (in part or whole) to be adopted by another national, regional, or international organization? ? Do not know at this time

Technical Committee Name and Number:

Contact person:

Contact person Phone Number:

Contact person Email Address:

7.3 Will this project result in any health, safety, security, or environmental guidance that affects or applies to human health or safety? No

7.4 Additional Explanatory Notes:

Scope and Purpose of the Modified PAR have been edited to better match the focus of the working group and to reflect the goal of this standard development more precisely. The working group felt this was necessary in order to ensure that the Scope and Purpose stated in the PAR matches the Scope and Purpose of the draft document intended for submission for ballot.

8.1 Sponsor Information:

Is the Scope of this project within the approved scope/definition of the Sponsor's Charter? Yes

If no, please explain: